CHAPTER 13. POWER ELECTRONICS: POWER AMPLIFIERS

13.1. POWER DISSIPATION AND THERMAL MANAGEMENT

When appreciable levels of power are to be handled by circuits and devices the design and analysis is shifted to the thermodynamic side of electronics. This context is represented by figure 13.1. The voltage rails then are the energy source and the load ($R_L$) is where we want the energy to go. The circuit is then a conduit for the flow (in Joules/sec). The input should be assumed to be a negligible contributor to the power and requires itself as a control node only.

![Figure 13.1-1. Thermodynamic context of power amplifier.](image)

As represented by the figure the power flow is

$$P_S = P_L + P_D \quad (13.1-1a)$$

And design is oriented toward the efficiency, which is fraction of the power delivered to the load.

$$\eta = \frac{P_L}{P_S} \quad (13.1-1b)$$

An efficiency of 100% would be nice except that it violates the 2nd law of thermodynamics. But we do push for designs that are close. We also have much concern about the power $P_D$ dissipated in the circuit. Power dissipated in the circuit causes heating. Heat degrades the circuit capabilities and operational lifetime of the devices. In excess it will cause metallurgical changes that damage the transistors. And so a part of the design analysis is framed around the thermal attitudes of the transistors.
Transistors are also not that linear over wide-swing operation. Furthermore the circuit has compliance limits imposed by the power supply rails. So for the sake of distortion reduction, symmetric design topologies are preferred, as indicated by the bipolar \((+V_S, -V_S)\) voltage rails of figure 13.1.

The transistor has an internal thermal resistance. The power dissipated within a semiconductor device is a consequence of Joule heating and will fall along the electrical conducting path. Since semiconductor devices usually include a junction the internal heating is referenced to a junction temperature \(T_J\). The temperature difference between \(T_J\) and the the external ambient temperature \(T_A\) (air) is expected to be proportional to the dissipated power, for which we might expect

\[
T_J - T_A = \theta_J P_D
\]  

(13.1-2)

where \(P_D\) = power dissipated in the device. The constant of proportionality \(\theta_J\) is defined as the ‘thermal resistance’ between junction and the ambient (air). It may also go by the nomenclature \(R_{th}(JA)\). Thermal resistance is given in terms of °C/W. The lower the thermal resistance, the more quickly heat can be conducted away from the junction. Cooler junctions are happier junctions. And they also live longer.

Transistors have a maximum rated junction temperature, \(T_A(\text{max})\), on the order of 150 to 200 °C. \(T_A(\text{max})\) which should not be exceeded, or irreversible metallurgical effects, distortion of the space-time continuum, or something else equally undesirable will take place. One of the design requirements is that \(T_J\) be kept \(<\ T_A(\text{max})\).

![Figure 13.1-2 Thermal resistances.](image)

Temperatures can be kept healthy if the transistor is given a good thermal conduction path from the junction to the ambient. Since the ambient environment is usually air, the exterior part of the thermal path will usually be in the form of a ‘heat sink’ radiator, usually little more than a metal plate with fins. As indicated by figure 13.1-2, the thermal resistance \(\theta_J\) between the junction and the ambient medium consists of a series of heat-conducting layers, each of which have their own thermal resistance, so that

\[
\theta_J = \theta_{JC} + \theta_{CS} + \theta_{SA}
\]

where \(\theta_{JC}\), \(\theta_{CS}\), and \(\theta_{SA}\) are the thermal resistances of the various layers between the junction and the ambient, consisting of junction-to-case, the case-to-sink, and the sink-to-ambient, layers (or elements)
respectively. Take note of the definitive subscripts. Default for ambient $T_A$ is 25°C. In a demanding environment the ambient temperature $T_A$ will likely be a mil spec requirement $-55\, ^\circ\text{C} < T_A < 125\, ^\circ\text{C}$.

Junction-to-case thermal resistance, $\theta_{JC}$, is defined by the power rating of the transistor. The power rating $P_D(\text{rated})$ is the power at which the transistor reaches its limit temperature $T_J(\text{max})$ when the device is test mounted on a humongous heat sink. And from this context we may obtain junction-to-case thermal resistance

$$\theta_{JC} = \frac{(T_J(\text{max}) - 25)}{P_D(\text{rated})} \quad (13.1-3)$$

(Note: case reference temperature $T_C$ is defaulted at 25°C). This assessment is often where we start since it defines the basic limit of the power transistor. The internal junction-to-case resistance, $\theta_{JC}$, is typically on the order of 1 to 10 °C/W, depending on the power rating of the transistor, e.g. the TIP31C which is a general-purpose 40W transistor with $T_J(\text{max}) = 150\, ^\circ\text{C}$ would have a $\theta_{JC}$ of $3.13\, ^\circ\text{C/W}$ according to equation (13.1-3).

Thermal resistance $\theta_{CS}$ is the contact resistance between the case of the device and the heat sink, usually identified by a (modest) use of ‘heat sink grease’, typically on the order of 0.1 to 0.5 °C/W.

The sink-to-ambient or heat sink resistance, $\theta_{SA}$, depends on construction and size of the heat sink. A typical heat sink with radiative fins should have a reasonably low thermal resistance per length. Doubling of the size of the heat sink will approximately halve its thermal resistance.

Consider the following example:

**EXAMPLE 13.1-1:** A pair of TIP31C 40W transistors are used for a class-A amplifier and have need to handle a dissipation total of $P_D = 20\, ^\circ\text{C}$. According to the specification sheet, $T_J(\text{max}) = 150\, ^\circ\text{C}$ and heat sink grease such that $\theta_{CS} = 0.15\, ^\circ\text{C/W}$,

(a) what heat sink thermal resistance $\theta_{CS}$ is needed to keep junction temperature $T_J < 135\, ^\circ\text{C}$

(b) what size heat sink is needed, assuming that a 2 cm length of stock has $\theta_{SA} = 16\, ^\circ\text{C/W}$?

**SOLUTION:** The internal thermal resistance, for $T_C = 25\, ^\circ\text{C}$ (= default) will be

$$\theta_{JC} = (150 - 25)/40 = 3.13\, ^\circ\text{C/W}$$

Each transistor must dissipate 10W, and with the junction requirement of $T_J \leq 135\, ^\circ\text{C}$

$$\theta_{JA} = (T_J - T_A)/P_D = (135 - 25)/10 = 11.0\, ^\circ\text{C/W}$$
Therefore (a) a heat sink of thermal resistance

\[ \theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS}) = 11.0 - (3.15 + 0.15) = 7.7 \, ^\circ\text{C/W} \]

is required for each transistor. (b) Using the heat sink stock cited, which is 16 \, ^\circ\text{C/W} for each 2 cm, each heat sink must be of length

\[ l = \frac{16}{7.7} \times 2\text{cm} = 4.1\text{ cm} \]

For extra margin a 4.5 cm piece of stock might be cut off for each transistor.

If we do not have heat sink bar stock we would probably go to catalog resources. Since the TIP31-C has a TO-220 case, it might be fortified by a thermalloy TO-220 black anodized, at 13\,^\circ\text{C/W}.

We also might elect a limit on the power dissipated by a given transistor in terms of a safety margin for which \( P_D < P_D(\text{max}) \). And since \( P_D = I_D \times V_D \), this represents a hyperbola in the \( I_D \) vs \( V_D \) domain. As a nomenclature \( I_D \) is the current through the device and \( V_D \) is the voltage across the device,

The power hyperbolas for BJT and FET devices are represented by Figure 13.1-2. Electrical properties of a device are represented by \( I_C \) vs \( V_{CE} \) for the BJT and by \( I_D \) vs \( V_{DS} \) for the FET. For circuit design, these graphics also are used in conjunction with load lines, etc. If we overlay a power limit on the device characteristics it is then represented by the hyperbolic (constraint) \( P_D(\text{max, de-rated}) = I_D \times V_D \). \( P_D(\text{max, de-rated}) \) includes the de-rating effect of the heat sink.

![Figure 13.1-2 Maximum power hyperbolae for power transistors](image)

It should be noted that it is unrealistic to expect a 40W transistor to dissipate 40W because of the thermal path de-rating and the safety margin.
EXAMPLE 13.1-2: A TIP31C 40W transistor has $T_J(\text{max}) = 150^\circ\text{C}$. If it is mounted on a (relatively large) heat sink with $\theta_{CA} = 2.12^\circ\text{C/W}$, and it is desired that it operate with safety margin $\Delta T_J = 20^\circ\text{C}$, then what is the maximum (de-rated) power $P_D$ that it can dissipate?

SOLUTION: The internal thermal resistance, for $T_C = 25^\circ\text{C}$ (= default) will be (like Example 13.1-1)

$$\theta_{JC} = \frac{(150 - 25)}{40} = 3.13^\circ\text{C/W}$$

The total thermal resistance is then

$$\theta_{JA} = \theta_{JC} + \theta_{CA} = 3.13 + 2.12 = 5.25^\circ\text{C/W}$$

The maximum power that can be dissipated is then

$$P_D = \frac{[(T_J(\text{max}) - \Delta T_J) - T_J]}{\theta_{JA}} = \frac{[(150 - 20) - 25]}{5.25} = 20.0\text{W}$$

Which tells us that the de-rated capability is typically only about 50% that of the rated 40W.

13.2 LINEAR POWER AMPLIFIERS

In most applications involving signal amplification the final stage of the circuit is an output driver to a large transducer, usually electromechanical or radiative. One of the more typical transducers is the audio speaker, which is effectively an electromagnetic air piston. Load transducers like the audio speaker come in various sizes ranging from little pipsqueaks to giants capable of defoliating trees along the roadway. So in like manner power circuits must be constructed in various sizes matched to the demands of the output transducer. For simplicity we generalize the load transducer as (load) resistance $R_L$.

It should be noted that the power an amplifier delivers to an output transducer is drawn directly from the power supply rails. The ‘amplifier’ circuit acts to channel power to the output load and is little more than a pair of power transistors deployed between load and the power rails. Most of the time we assume that the control signal is sinusoidal and that the transistors will then pass a sinusoidal current to the load. In some topologies we let the transistors act as switches with an output that is a rail-to-rail square-wave.

For a sinusoidal signal of amplitude $V_L$ and load resistance $R_L$ the time average of the power $P_L$ to the load will give
\[
\langle P_L(t) \rangle = \frac{1}{T} \int_0^T \frac{1}{R_L} [V_L \sin(\omega t)] \, dt = \frac{V_L^2}{R_L} \times \left( \frac{1}{2\pi} \int_0^{2\pi} (\sin^2 \theta) \, d\theta \right) = \frac{1}{2} \frac{V_L^2}{R_L}
\]

(13.2-1)

For purposes of simplicity equation (13.2-1) is taken as a default. Any other waveforms can be assessed in terms of added harmonics. Assuming a clean sinusoidal signal and bipolar power rails the power delivered to a transducer by the drive transistors cannot be any more than

\[
P_L \text{ (upper limit)} = \frac{1}{2} \frac{V_S^2}{R_L}
\]

(13.2-2)

where rails of opposite polarity \( V_S \) are assumed. Therefore the first step in analyzing a linear power amplifier is to determine the power supply requirements needed to support the output transducer at the desired load level.

For purposes of matching application to circuit form, power amplifiers are usually identified by a classification system. Classification is defined by the duty cycle of the drive transistors. A circuit for which the drive transistors are always conducting (100% duty cycle) is called a class-A amplifier. Class-A amplifiers provide a nearly undistorted output signal but do so at miserable efficiency. Most casual circuits are of type class-A since they operate about an “operating point” level. For the class-A amplifier the efficiency and the level of power dissipated in the transistors are at their worst when the amplitude of the input signal is zero, since then all of the power will then be dissipated in the circuit.

We improve the efficiency dramatically if we use a circuit topology which is non-conducting when the signal level is zero. We can accomplish this easily if we employ a pair of complementary transistors to drive the load. Ideally, each of the drive transistors conducts only for half of the cycle and are off for the other half cycle. This type circuit is called a class-B amplifier. Each of the drive transistors in a class-B amplifier have duty cycle of 50%. When the signal is at zero amplitude neither device is conducting and no power is consumed.

If the circuit is modified so that the drive transistors have a duty cycle slightly more than 50%, then the circuit is called class-AB. Class-AB circuits have an efficiency slightly less than the class-B amplifier. Class-AB amplifiers resolve a zero-crossing distortion problem that afflicts class-B amplifiers.

Class-C amplifiers’ operation uses drive transistors biased below cutoff, which conduct only for a small fraction of a cycle and therefore have a duty cycle less than 50%. They are used only for tuned circuits. Typical application is of the form of the modulation circuit for an RF receiver or transmitter. They can have an efficiency greater than class-B and may approach 100% for a highly resonant circuit.

A type amplifier that does not quite fit the duty-cycle classification pattern is the class-D amplifier. Class-D amplifiers are switching amplifiers, and their efficiency can approach 100%. The class-D amplifier must include a modulator at the front-end to translate the waveform into high-frequency pulse widths and a filter network at the back end to remove the high-frequency pulses from the amplified output. Usually the filter network is of a simple, lossless R-L or R-C form.
Table 13.2-1 summarizes the different types of common power amplifiers and the way in which the signal is handled.

Table 13.2-1. Power amplifier classes:

<table>
<thead>
<tr>
<th>TYPE</th>
<th>DUTY CYCLE</th>
<th>WAVEFORM</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLASS A</td>
<td>D = 100%</td>
<td><img src="image" alt="Waveform" /></td>
</tr>
<tr>
<td>CLASS B</td>
<td>D = 50%</td>
<td><img src="image" alt="Waveform" /></td>
</tr>
<tr>
<td>CLASS AB</td>
<td>D &gt; 50%</td>
<td><img src="image" alt="Waveform" /></td>
</tr>
<tr>
<td>CLASS C</td>
<td>D &lt; 50%</td>
<td><img src="image" alt="Waveform" /></td>
</tr>
<tr>
<td>CLASS D</td>
<td></td>
<td><img src="image" alt="Waveform" /></td>
</tr>
</tbody>
</table>

13.3 POWER TRANSISTORS

Power transistors are the big strong slow members of the transistor kingdom. They often live in their own separate packages with a tab or baseplate designed to have contact with a heat sink. They are not formed in the same way as their integrated-circuit cousins. Therefore power transistors are not usually included in an integrated circuit, since most IC fabrication technologies are dedicated to high-density, mild-
temperature applications. This exclusive context is not a law, and developments of new technologies have allowed us to embed large transistors in integrated circuits, with some qualification.

Whether in separate or integrated form, we should think of power transistors and power diodes as the heavy lifters of the semiconductor kingdom, designed to handle great power levels and packaged to dissipate great levels of heat.

In order to design for best performance and operating lifetime of power transistors, it is appropriate to take a critical look at their operating and performance characteristics.

In the first place, we expect power transistors to have relatively large cross-sectional area. Naturally, if all they had to do was handle larger currents, we would form a large transistor of the usual type. But higher levels of power also imply that we need to control higher voltage levels without a breakdown disaster. So, in general, power transistors are constructed with a different semiconductor layering, usually including one or more lightly-doped regions which have the ability to accommodate higher voltage levels without suffering breakdown. Power transistors and diodes are thus characterized by:

(a) greater cross-sectional area
(b) a relatively thick, lightly-doped junction layer, for reduced level of E-field

There are other, more subtle things that we may do as well, such as heavy doping with gold or copper to speed-up the recombination processes. For MOS devices, thicker oxide layers are necessary to protect the device from overvoltages which causes the threshold, $V_{TH}$, to be higher.

These modifications will compromise some of the other characteristics that we covet, such as low resistance and fast response. Lightly doped regions result in significant intrinsic resistance along the current path. Greater areas imply larger capacitances. Larger current levels imply higher levels of injected and stored charge. These effects are all bad for switching speed and internal power dissipation.

Power transistors are therefore characterized by the following performance limitations:

(c) higher $V_{TH}$, lower $\beta_F$ (also called $h_{FE}$)
(d) slower switching speeds
(e) greater $V_{CE(sat)}$, $V_{DS(sat)}$
(f) greater intrinsic resistance in the conducting path

We will take a short look at each of the most common types of power transistors and components, and assess them as candidates for our power electronics circuits.

**pin junctions**: The $p-i-n$ junction is a $pn$ junction with a layer in the middle that is intrinsic or nearly-intrinsic semiconductor. To the semiconductor world it probably looks like an ice-cream sandwich, with the (vanilla) core being nearly ‘clean’ of impurities. Actually, the core is always slightly doped, so we usually call the junction a $p-\pi-n$ if the "intrinsic" layer is slightly p-type, or a $p-\nu-n$ junction if the "intrinsic" layer is slightly n-type. Figure 13.3-1 shows a representative *pin* junction and E-fields thereto.
The figure shows that, in reverse-bias, the E-field is relatively low, since the intrinsic layer can be made of thickness much larger than the usual micron thickness depletion depth of the typical \( p-n \) junction. The E-field is approximately

\[ E \approx \frac{V_J}{W} \]  \hspace{1cm} (13.3-1)

where \( V_J \) is the junction reverse-bias and \( W \) is the thickness of the intrinsic layer. Junction breakdown typically takes place at 20 to 40 V/\( \mu \)m, so a reverse-bias of 100 V across an intrinsic layer thickness of 10\( \mu \)m still has a comfortable safety margin.

However in forward bias, we are faced with an intrinsic region across the main current path that has a miserable conductivity, \( \sigma = \mu N_i \) for which \( N_i \) is the (low) doping density and \( \mu \) is carrier mobility. For cross-sectional area \( A_i \) and layer thickness \( W_i \), this leaves the device with series resistance

\[ R_i = \frac{W_i}{q\mu N_i A_i} \]  \hspace{1cm} (13.3-2)

**EXAMPLE 13.3-1:** Determine the intrinsic resistance for a silicon \( p-n \) junction of cross-sectional area \( A_i = 1.0 \text{ cm}^2 \), doping of the intrinsic layer \( N_i = 2 \times 10^{14} \#/\text{cm}^3 \) and layer thickness \( W_i = 30 \mu \text{m} \). Assume \( \mu_n = 1250 \text{ cm}^2/\text{Vs} \).

**SOLUTION:**

\[ R_i = \frac{W_i}{q\mu N_i A_i} = \frac{30 \times 10^{-4}}{(1.6 \times 10^{-19}) \times 1250 \times (2 \times 10^{14}) \times 1.0} = 75 \text{ m\Omega} \]

As resistances go, this doesn’t sound too bad, until you realize that this junction may be conducting 100 A over a 50% duty cycle, in which case it must dissipate...
At this level of internal power dissipation this had better be one tough junction.

In forward bias we also have something of a response problem, due to the fact that the intrinsic region is flooded with charge carriers. And as a result of the low doping levels, we will not necessarily have a fast recombination time constant since recombination time depends on the density of impurity sites. Gold or copper is usually added to enhance recombination, but this type of doping causes other complications. When bias voltage is swung from forward to reverse, current will continue to flow with time constant determined (approximately) by the diffusion capacitance per area,

\[ C_D = J_D \tau_R \]  \hfill (13.3-3)

where \( J_D \) is the forward current density and \( \tau_R \) is the recombination time constant, which is usually on the order of \( \mu s \). Adding to our grief, we also will usually have large-area (and consequently large capacitance) junctions.

**Power BJTs:** The power BJT is little more than a conventional BJT with a collector junction of the form of a \( p-i-n \) junction rather than the usual simple \( pn \) junction. We see this represented by figure 13.3-2.

Sometimes we can get away with a ‘normal’ BJT construction and simply have a mildly-reduced doping level for the collector material. As long as we don’t have any reverse junction biases in excess of 100V, this will probably work OK, but we do have to make the device with a larger than normal base-width (layer thickness) to avoid ’punch-through’ problems. Transistors of this species will usually have a \( \beta_F \) \((h_{FE})\) somewhat less than the traditional BJT, on the order of 25 to 50.

Higher-power BJT transistors, which must be able to withstand reverse junction biases in excess of 200V, are typically of the form represented by figure 13.3-2. This figure shows a BJT with an \( n^+ - p - n^+ \) construction. The lightly-doped region is usually called the *drift-region* since the carriers must ’drift’ across this region before they get ‘collected’ at the \( n^+ \) collector. Transistors of this type are lucky to have forward current gain \( \beta_F \) as good as 25. They are also characterized by a large ‘quasi-saturation’ region of operation, corresponding to partial forward-bias conditions in the lightly-doped drift region, as represented by figure 13.3-2(c)
High-power BJT transistors, as represented by figure 13.3-2(b), are therefore also characterized by a fairly poor $V_{CE}(sat)$ because of this quasi-saturation region.

This effect is represented by figure 13.3-2(a) and (b). If we analyze details of the semiconductor junction work-functions and injected carrier levels, we will find, after all the mathematical and semiconductor dialogue is completed, that the power BJT structure will have a $V_{CE}(qsat)$ at the boundary of the quasi-saturation region given by

$$V_{CE}(qsat) = V_{BE} - 2V_T \ln \left(\frac{N_i}{n_i}\right) + V_i$$  \hspace{1cm} (13.3-4)

where $V_i = R_c \times I_C$ is the resistive drop in the intrinsic region, $V_{BE}$ is the voltage across the forward-biased base-emitter junction, and the term $2V_T \ln(N_i/n_i)$ is a collective term due to the work function potential between base and intrinsic regions and the charge carriers injected into the intrinsic region from the base. The term $n_i = intrinsic\ carrier\ density$ for a pure semiconductor, which $= 1.5 \times 10^{10} \#/cm^3$ for the most likely semiconductor, silicon, at nominal ambient temperature 300 K. $V_T$ is the thermal voltage, and is approximately .026V at 300K

**EXAMPLE 13.3-2:** Assume that a 400V power BJT has a pin collector junction of the same dimensions and doping as example #13.3-1. For a $V_{BE}$ of 0.69 V and current density $J = 50A/cm$, find the value of $V_{CE}$ at the boundary of quasi-saturation.

**SOLUTION:** This is a good-sized transistor so don’t expect a small $V_{CE}$. At the boundary of quasi-saturation,

$$2V_T \ln(N_i/n_i) = 2 \times .026 \times \ln[(2 \times 10^{14})/(1.5 \times 10^{10})] = 0.494V$$
so that the complete $V_{CE}$ across the BJT at the onset of the quasi-saturation condition will be

$$V_{CE(qsat)} = V_{BE} - 0.494 + R_i \times (J \times A_i) = 0.69 - 0.494 + (0.075 \times 50) = 3.95\text{V}$$

At saturation conditions, for which base current is large, the pin junction becomes forward-biased and carriers will flood the intrinsic region and make $R_i$ approximately 0.0. In this case

$$V_{CE(sat)} = 0.69 - 0.494 = 0.195\text{V}$$

In practice, $V_{CE(sat)}$ is seldom achieved for a high-power transistor, because the forward current gain $\beta_F$ of such a transistor is so low it becomes difficult to provide the necessary base current. Even in the active region, $\beta_F$ would probably be no better than about 20 for a transistor of this power capability.

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**The Power MOSFET:** The power MOSFET is a vertical structure as represented by figure 13.3-3. A power nMOSFET is represented. It is a double-diffused structure (sometimes called DMOS). In this case the DMOS is formed by a p-well diffused into a lightly-doped substrate layer, followed an n$^+$ source diffused into the p-well. Although this structure doesn’t look much like the classical MOSFET, the figure shows that the region of the p-diffusion at the surface will be subject to an E-field across the oxide at that point. Gate-inspired field inversion will be achieved in the p-material and conduction will occur. The drain terminal is at the bottom. High voltages at the drain node are isolated from the gate and the implants at the upper surface by the “thick” lightly-doped (n$^-$) substrate layer.

![Image of power MOSFET](image)

**Figure 13.3-3** The power MOSFET:
(a) cross-sections  (b) $I_D$ vs $V_{GS}$ characteristics  (c) $I_D$ vs $V_{DS}$ output characteristics.
In reverse bias the intrinsic layer provides the usual high-field protection by means of the pin junctions. In forward bias the intrinsic layer has a finite series resistance that will give undesirable loss effects not unlike those for the power diode and the power BJT. The MOSFET gate-channel voltage must be able to withstand channel bias levels on the order of 10 to 20 V, and therefore requires oxide thickness on the order of 100 to 200 nm. The p-well must be at a healthy doping level to avoid a problem called 'punch-through'. These effects combined imply that $V_{TH}$ will have a magnitude on the order of 4 to 5 V. Because the depletion region extends into the channel during forward operation, the value of $L$ is small. This short-channel results in very strong field along the channel which drives the transistor into a velocity-saturation mode of $V_{DS}$ when in the forward active mode. The result is a linear transfer characteristic for $I_D$ vs $V_{GS}$, as represented by figure 13.3-3(b), and is of the form

$$I_D = W\mu C_{OX} v_C (V_{GS} - V_{TH})$$  \hspace{1cm} (13.3-5)$$

In velocity saturation $v_C$ is on the order of $10^7$ cm/s for electrons in silicon. $C_{OX}$ is the oxide capacitance/area and $W$ is the channel width, which we make as large as possible by artful designs of the surface geometry. One of the favored surface designs is a hexagonal arrangement, and such structures are therefore called HEXFETS.

Resistance $r_{DS}$ is the channel resistance for a MOSFET at low $V_{DS}$, given by

$$r_{DS} = \mu C_{OX} \frac{W}{L} (V_{GS} - V_{TH})$$  \hspace{1cm} (13.3-6)$$

and represents the lower boundary of the velocity-saturated drain levels, as shown by figure 13.3-3(c). It also represents the drain resistance of the MOSFET channel when it is operating in its most conductive state for which power dissipation in the device may be identified.

### 13.4 Class-A Amplifiers

A class-A power amplifier can be of any topology for which the transistor is biased into a quiescent point for amplification and control but is most accurately represented by the voltage-follower circuit as represented by figure 13.4-1(a). Since the transistor is biased in the active regime the drive transistor will be in a mode with a 100% duty cycle. In the voltage follower mode the drive transistor stays in the active mode throughout the drive cycle. The output should therefore be almost undistorted, depending only on the linearity of the drive transistor(s). The follower circuit has a fairly linear response over a wide output range, as indicated by figure 13.4-1(b). Therefore the class-A circuit suffers relatively little distortion of the output. The current source, which defines fixed current $I_S$, is also a power transistor.
The voltage follower circuit does not necessarily have to make use of bipolar power rails but is elected in this case for comparisons to other classes of power amplifiers for which bipolar power rails are required. Voltage and current specifications of the circuit design are defined in terms of the $P_{L\text{(max)}}$ delivered to load $R_L$. For a power amplifier with BJT drivers, and assuming that the output driver of the current source is a single BJT, then the amplitude of the output waveform will be bounded by the voltage rails $\pm V_S$ offset by $V_{CE\text{(sat)}}$. To first-order rough, $V_{CE\text{(sat)}}$ is assumed negligible for all but the lower voltage demand ($V_L < 5\text{V}$) levels. For high-power, high-voltage BJTs, the $V_{CE\text{qsat}}$ limit may be as much as $5\text{V}$, but even this higher limit may also be ignored for drive voltage levels on the order $V_L > 100\text{V}$, typical for high-power transistors.

The approximate and appropriate current level needed to supply the load $R_L$ is then

$$I_S = \frac{V_L}{R_L} \quad (13.4-1)$$

This current is also the quiescent current corresponding to input signal of zero amplitude. Since $I_S$ is a fixed level then the power supply will continuously deliver power at the level

$$P_S = 2V_S \times I_S = \frac{2V_S^2}{R_L} \quad (13.4-2)$$

From previous analysis, sinusoidal signals of amplitude $V_L$ at $R_L$ will deliver average power of

$$P_L = \frac{1}{2} \frac{V_L^2}{R_L} \quad (13.2-1)$$

which is a maximum = $P_L\text{(max)}$ when $V_L = V_S$.

From the efficiency relationship $\eta = P_L/P_S$ then that for the class-A topology is
\[
\eta = \frac{P_L}{P_S} = \frac{V_S^2}{2V_L^2/R_L} = \frac{1}{4} \frac{V_L^2}{V_S^2}
\] (13.4-3)

with maximum efficiency \(\eta_{\text{MAX}} = 25\%\) and only then if \(V_L \rightarrow V_S\).

Otherwise the circuit design should target the worst case power dissipation. Worst case occurs at quiescent with \(V_L = 0\) and all of the power is then dissipated in the transistors, i.e.

\[
P_D(\text{worst}) = P(\text{supply}) = \frac{2V_S^2}{R_L} = 4P_L(\text{max}) \quad (13.4-4)
\]

The thermal management system (heat sinks, etc) should be roughly appropriated in terms of \(4P_L(\text{max})\).

The action of the transistors for the class-A amplifier is represented by figure 13.4-2.

**Figure 13.4-2** (a) Class-A circuit consisting of BJT driver and simple current mirror. (b) Waveforms for the class-A amplifier.

If the transistors have individual (top-hat) cooling systems, each should be defined in terms of half the worst-case dissipation, or approximately \(2 \times P_L(\text{max})\).

Specifications of design will usually cite values for \(R_L\) and \(P_L(\text{max})\). Design is then a matter of identifying power supply requirement \(V_S\) and selecting the power ratings for the transistors and appropriate design choices for their heat sinks.

Consider the following example:
EXAMPLE 13.4-1: It has been determined that mosquitoes are susceptible to certain audio frequencies for which they will fall out of the sky, lie on their backs, and wave their little legs in appreciation. The piezoelectric oscillator that does this operates at maximum effectiveness when $P_L = 4W$. The equivalent load resistance of this transducer is $R_l = 10\Omega$ and is to be driven by a class-A amplifier of the form of figure 13.4-2. Transistor Q3 is 1/5 the size of Q2. Determine

(a) power supply requirements $V_S$, $I_S$ and $P_S$ of the voltage rails and
(b) load efficiency for fixed input oscillator at amplitude $V_I = V_S$.

SOLUTION: Maximum power to the load results when $V_L = V_S$. So for $P_L = P_L_{(max)} = 4W$ and using equation (13.4-4)

$$V_S = \sqrt{2P_L_{(max)}R_L} = \sqrt{2 \times 4 \times 10} = 8.94V \approx 9.0V$$

for which the current mirror must source at least

$$I_S = \frac{V_S}{R_L} = \frac{8.94}{10} = 0.9A$$

For a simple current mirror, as shown, the biasing resistance $R_i$ should be

$$R_i = \frac{9.0 - 0.7}{0.9} = 92\Omega$$

The positive supply rail must provide $P_{S1} = I_S \times V_S = 2 \times 8W = 8W$. The negative supply rail must provide current of approximately $(I_S + I_S/5) = 1.07A$ so that $P_{S2} = (-1.07) \times (-8.94) = 9.6W$.

For fixed $V_I = V_S = 9.0V$, the efficiency appropriate to this design would be

$$\eta = \frac{P_L}{P_{S1} + P_{S2}} = \frac{4}{8 + 9.8} = 0.225 \quad (22.5\%)$$

A minor caveat of this circuit is that the input and output signals for this amplifier are offset from one another by approximately 0.7 V. For optimum performance and minimum distortion the offset should be accommodated by a 0.7V level shift in the signal provided by the stage preceding the power amplifier.
13.5 CLASS-B AMPLIFIERS

The class-A amplifier is a poor choice of a power amplifier since it consumes power when in the quiescent \((V_L = 0)\) state. Consequently if you value your battery power supply you will totally avoid the class-A amplifier. In defense of class-A and the community of crazy-man hardcore audiophiles class-A amplifiers are very linear and therefore are of the highest quality. But most linear power amplifiers are designed using the class-B form or its cousin class-AB for which the conduction path between voltage rails is cut off, or nearly so, when there is no input signal.

In order to achieve such a caveat, class-B makes use of complementary drive transistors with each at a 50% duty cycle as shown by figure 13.5-1. At the most basic level a complementary \(npn\) and \(pnp\) BJT pair is the load driver stage. Class-B circuits are also identified as push-pull amplifiers because of the directions of ‘push-pull’ flow of current through the load \(R_L\). In this respect a similarity exists between the class-B action and that of the class-A circuit topology, except that zero \(V_L\) (quiescent state) corresponds to no conduction path between the voltage rails.

\[\text{Figure 13.5-1 Class-B topology with complementary push-pull BJTs}\]

For ideal class-B the transistors conduct at a 50% duty cycle and the time-averaged current that is drawn from (either) rail of the power supply will be:

\[
\langle I(t) \rangle = \frac{1}{2\pi} \int_0^\pi V_L \sin \theta \frac{d\theta}{R_L} = \frac{V_L}{R_L} \times \frac{1}{2\pi} \int_0^\pi \sin \theta d\theta = \frac{1}{\pi} \frac{V_L}{R_L} \tag{13.5-1}
\]

assuming sinusoidal signals. Therefore the power drawn from the voltage rails is

\[
P_s = I_{AV} \times 2V_s = \frac{2V_L V_S}{\pi R_L} \tag{13.5-2}
\]
Assuming sinusoidal signal the power to the load is the same as that given by equation (13.2-1)

\[ P_L = \frac{1}{2} \frac{V_L^2}{R_L} \]  

(13.2-1)

For which the efficiency \( \eta = P_L/P_S \) will be

\[ \eta = \frac{P_L}{P_S} = \frac{V_L^2 / 2R_L}{2V_LV_S/\pi R_L} = \frac{\pi V_L}{4 V_S} \]  

(13.5-3)

The maximum power is delivered to the load at \( V_L = V_S \) which gives a (theoretical maximum) efficiency \( \pi/4 \), or 78.5\% for the ideal class-B topology.

The more definitive relationship makes use of an assessment of \( P_D \) vs \( V_L \), defined by equations (13.5-2) and (13.2-1), for which

\[ P_D = P_S - P_L = \frac{2V_LV_S}{\pi R_L} - \frac{1}{2} \frac{V_L^2}{R_L} \]  

(13.5-4)

Via (Excel) spreadsheet this relationship is shown by figure 13.5-2.

![Class B power dissipation](image)

**Figure 13.5-2.** For purposes of plot analysis \( V_S = 10\) V. By inspection it appears that \( V_L \) (worst) is \( \cong 6.4\) V, which is confirmed by equation 13.5-5 (below).

Equation (13.5-4) is quadratic in \( V_L \) with maximum (= worst-case) dissipation when \( \partial P_D/\partial V_L = 0 \), for which

\[ V_L = \frac{2V_S}{\pi} \equiv V_{LWC} \]  

(13.5-5)
Substituting (13.5-5) into (13.5-4) the maximum power (= worst-case) dissipated in the circuit will be

\[ P_D(\text{worst}) = \frac{2}{\pi^2} \frac{V_S^2}{R_L} = \frac{4}{\pi^2} \times \frac{1}{2} \frac{V_S^2}{R_L} = \frac{4}{\pi^2} P_L(\text{max}) \approx 0.406 P_L(\text{max}). \]  

(13.5-6)

For an optimized system \( V_S \) is the same as \( V_L(\text{max}) \) and thereby serves as a reference point.

\( V_{LWC} \) is also another reference point. When this voltage is inserted into equation (13.5-3) the result is an efficiency \( \eta = 50\% \). Efficiency \( \eta = 50\% \) also corresponds to the case in which \( P_D \) and \( P_L \) are equal.

Worst-case power dissipation is always invoked in the analysis and design of the thermal management system. So equations (13.5-5) and (13.5-6) are critical benchmarks for class-B circuits.

Power amplifier design is usually specified for a given \( P_L(\text{max}) \). Since \( P_L \) is sourced by \( P_S \) it follows that the \( V_S(\text{min}) \) rail voltage will be.

\[ V_S(\text{min}) = V_L(\text{max}) = \sqrt{2R_L P_L(\text{max})} \]  

(13.5-7a)

This equation is applicable whether for class A or class B or (later) class AB.

Since rail voltages should uniformly be higher than \( V_L(\text{max}) \) then \( V_L \) may be closer to \( V_{LWC} = 2V_S/\pi \) and it is more likely that a class-B circuit will have an efficiency closer to 50% than 78%.

The condition that defines \( V_S(\text{min}) \) can also be used to define a minimum load level \( R_L \)

\[ R_L(\text{min}) = \frac{V_S^2}{2 \times P_L(\text{max})} \]  

(13.5-7b)

which also defines an \( I_L(\text{max}) = V_S/R_L(\text{min}) \).

13.6 DISTORTION

Distortion is an electronic fact of life. The class-B topology suffers from an effect called ‘cross-over’, when the output crosses zero and the signal is transferred from one device to the other. Non-linearity of the semiconductor devices causes distortion. Large amplitudes suffer from amplitude ‘flattening’ as the power rail limits are approached. All of these effects are part of a quantitative measure defined as the THD (total harmonic distortion).

Distortion is manifested by harmonics, for which the signal \( V_L(t) \) at the load will be of the form
\[ V_L(t) = V_1 \cos(\omega_1 t + \theta_1) + V_2 \cos(\omega_2 t + \theta_2) + V_3 \cos(\omega_3 t + \theta_3) + \cdots + V_N \cos(\omega_N t + \theta_N) \]

where \( \omega_1 \) is the frequency of the input signal. The frequencies \( \omega_2 = 2 \omega_1, \omega_3 = 3 \omega_1, \ldots \) etc are distortion harmonics accompanied by phase shifts, \( \theta_1, \theta_2, \theta_3, \ldots \) for which the rms output is

\[ V_{\text{rms}} = \sqrt{\sum_{n=1}^{\infty} \frac{V_n^2}{n}} \quad (13.6-1) \]

The ‘THD’ (total harmonic distortion) of \( V_L(t) \) is defined as

\[ \text{THD} = \frac{V_{\text{rms}}(\text{harmonics})}{V_{\text{rms}}(\omega_1)} = \sqrt{\sum_{n=1}^{\infty} \frac{V_n^2}{V_1^2}} \quad (13.6-2) \]

This equation represents the mathematics that is passed along to software. Distortion analysis is another of those tasks that the pspice domain is more than delighted to do since the software will decompose \( V_L(t) \) by invoking a Fourier-series analysis and even graph it if so desired. The result is a Fourier table and a THD generated and listed under the output file, as represented by example and figure 13.6-1.

**EXAMPLE 13.6-1:** Class-B amplifier with both crossover distortion and compliance limit distortion as assessed using SPICE.

**Figure 13.6-1:** Since \( V_a > V_s \), the output swing is clipped.

In assessing distortion the THD is the defining figure of merit even though we may single out some of the harmonic overtones. Clipping of the output (due to the compliance limits) results in distortion with a strong odd-harmonic content.
13.7 CROSS-OVER DISTORTION AND CLASS-AB

There is a little problem with the ideal class-B topology. A minimum $V_{BE}$ is necessary for a transistor to achieve active mode conduction. The class-B drive pair will therefore suffer a "dead zone" for inputs below this threshold, usually on the order of $-0.6V < V_I < 0.6V$ for a topology of the form of figure 13.5-1 the output will have a zero-crossing dead space. The effect is represented by figure 13.7-1.

Power BJT s are not atypically packaged as Darlington-pair s for which the dead zone is a factor of two worse. For the same reason, MOSFETs are not used in the voltage follower mode but in CS (common-source) push-pull topology since the cross-over effect is 3 to 4 times worse.

But have no cause to fear. The solution to cross-over is fairly simple, as represented by figure 13.7-2. The transistors are offset biased from one another so that the dead space is covered by the other transistor.
This puts each of the transistors in a duty cycle \( D \) slightly greater than 50%. This context is represented by figure 13.7-3.

![Figure 13.7-2. Class-AB diode bias of transistor pair](image)

Class-AB transistors have a duty cycle \( 50\% < D < 100\% \), or somewhere between class-B and class-A.

And usually the duty cycle \( D \) for class-AB is designed to be close to 50%. Therefore most of the analysis and design strategy associated with class-B are applicable to class-AB.

However at the quiescent condition \( (V_L = 0) \) a relatively small current \( I_Q \) must flow through the transistors. A bias network of form indicated by figure 13.7-2 is typical. Current source \( I_{bias} \) must be sufficient to supply the base drive and this gives the criterion

\[
I_{bias} > I_{B}^\text{(max)} = \frac{I_L^\text{(max)}}{\beta_F + 1}
\]

(13.7-1)
In order for effective class-AB operation, offset bias $V_{BB}$ must keep both transistor junctions in conduction at $V_L = 0$. This condition is typically achieved by stacking of as many diode bias junctions as there are transistor junctions. The use of junctions as the means to bias the junctions of the power transistors also avoids a destructive situation called thermal runaway. Thermal runaway avoids a fixed $V_J$ because, for fixed $V_J$, the current though the junction will approximately double for every $10 \, ^\circ\text{C}$ rise in temperature. The increase in junction current then causes an increase in temperature, and this produces an increase in current, which then causes an increase in temperature. The effect is exponential and catastrophic. When the bias $V_{BB}$ is set by (thermally linked) junctions as represented by figure 13.7-2, it will automatically compensate, with bias decreasing by $\Delta V = -2 \, \text{mV/}^\circ\text{C}$ as the biasing diodes heat up.

For a pair of BJT drive transistors the offset bias $V_{BB}$ is on the order of $2 \times 0.6 \, \text{V}$. More explicitly, $V_{BB} = V_{BE}(N) + V_{BE}(P)$ for the transistor pair. Taking inverses of the junction characteristics for which $I = I_S \exp(V_{BE}/V_T)$ for each transistors and assuming $I = I_S \exp(0.5V_{BE}/V_T)$ at quiescent, then retention of a relatively fixed $V_{BB}$ implies that

$$V_{BB} = V_T \ln(I_{EN}/I_S) + V_T \ln(I_{EP}/I_S) = 2 \times V_T \ln\left(\frac{I_Q}{I_S}\right)$$

For these relationships $I_S = \text{reverse saturation current of the output transistors, assumed to be matched,}$ and. $V_T = kT/q = \text{thermal voltage.}$

By inverting the logarithmic condition

$$I_Q^2 = I_{EN}I_{EP} \tag{13.7-2}$$

The currents $I_{EN}$ and $I_{EP}$ for the output transistors will be inverses of one another.

It is necessary to evaluate the current levels and device sizing concurrently. Otherwise there is little or no efficiency benefit. The problem is represented by example 13.7-1.

---

**EXAMPLE 13.7-1:** A class-AB amplifier configuration with biasing diodes 1/5 that of the drive transistor is used to drive an 8W, 4Ω load using matched complementary BJTs with $\beta_F = 50$.

Determine $I_{bias}$ and $I_Q$ under the requirement that current through the bias diodes $I_D$ is not allowed to vary by more than a factor of 10. For simplicity (and to avoid iteration) assume that $I_B(\text{min})$ is negligible $\approx 0$.

**SOLUTION:**

\[
I_{L(\max)} = \sqrt{2R_LP_L} = \sqrt{2 \times (4 \times 8)} = 8.0 \text{V} = V_{S(\min)}
\]

\[
I_D(\max) = \frac{8.0 \text{V}/4 \Omega}{2} = 2 \text{A}
\]

so $I_B(\max) = I_D(\max/\beta_F + 1) = 2 \text{A}/(50 + 1) = 39.2 \text{mA}$

\[
I_{Bias} = I_D + I_B \quad \text{so} \quad I_D(\max) + I_B(\min) = I_D(\min) + I_B(\max),
\]

\[367\]
Since \( I_D(\text{max}) = 10 I_D(\text{min}) \), and since \( I_B(\text{min}) \approx 0 \), then \( I_D(\text{min}) = 39.2 \, \text{mA} / (10 - 1) = 4.36 \, \text{mA} \)

Then \( I_D(\text{max}) = 10 I_D(\text{min}) = 43.6 \, \text{mA} = I_{\text{bias}} \)

\( I_D(\text{max}) \) = current through the diodes at quiescent. Since the diodes are 1/5 the size of the transistors then the \( I_Q \) through the transistor has to be

\[
I_Q = 5 I_D(\text{max}) = 218 \, \text{mA}
\]

This level of \( I_Q \) corresponds to quiescent power consumption

\[
P_Q = 2V_S \times I_Q = 3.48 \, \text{W}
\]

This is a heavy price to pay given that the \( P_D(\text{worst case}) \) for class-B is only \( 3.25 \, \text{W} \). Efficiency in this respect would then be

\[
\eta = \frac{P_L}{P_L + P_D + P_Q} = \frac{3.25}{3.25 + 3.25 + 3.48} = 32.5\%
\]

Take note that at \( V_L = (2/\pi)V_S \), \( P_L = P_D(\text{worst}) \)

The example indicates that an extra power \( P_Q \) must be added to the budget for correction of crossover distortion. The level can be considerably reduced if the biasing diodes are more nearly the same size (same power rating) as the output drive transistors. But this option also adds more bulk to the design.

The rest of the story, however, is the relative levels of current of the bias network (\( I_{\text{bias}} \)) to that of the output current. The relative levels are defined by the \( \beta_F \) of the output transistors. Unfortunately individual power BJTs have a relatively low \( \beta_F \), usually on the order of 25 to 50. Forward current gain is even less respectable for the PNP power BJT, since charge carrier mobility is about a factor of 2.5 lower for holes than it is for electrons.

However have no cause to fear. Because of these caveats, power transistors usually are devised as a Darlington (super-beta) pair, either in discrete form or in packaged form, as represented by figure 13.7-3. The Darlington pair has current gain

\[
\beta_F = \beta_1 \beta_2 + (\beta_1 + \beta_2)
\]

\[\text{Figure 13.7-3: The Darlington pair}\]
for which $\beta_f = 500$ to $10,000$. They are commonly packaged as a single unit and given the name super-beta transistors. Their large current gain is compromised by the fact that they also have an equivalent $V_{CE(sat)} = V_{BE1} + V_{CE(sat)} \approx 1.0V$. High-power, high-voltage transistors may have $V_{CE(sat)} = 5V$. The Darlington pair will also require an input offset biasing of $V_{BE1} + V_{BE2} \approx 1.2V$.

When we use a class-AB Darlington configuration, and even when we don’t, it is also convenient to use another input offset biasing scheme, the $V_{BE}$ multiplier circuit shown by figure 13.7-4. This circuit is a resistance defined ladder made up of $R_1$, $R_2$ and transistor $Q_5$ of the form represented by the figure. This circuit uses the junction $V_{BE1}$ of the bias transistor $Q_5$ as a reference voltage multiplied by the voltage ratio of $R_1$ and $R_2$ to get necessary $V_{BB}$ bias. Inasmuch as $Q_5$ is the reference junction for the input bias it is good form for it to have thermal contact with the output transistors in order to assure temperature compensation. A class-AB Darlington with $V_{BE}$ multiplier is shown by figure 13.7-5a.

A modification of the class-AB Darlington configuration for which the relatively weak PNP output driver is replaced is is shown by figure 13.7-5b. This topology is known either as the compound pnp or as the Sziklai configuration. Since the power transistor $Q_2$ is of type npn, the compound-pnp driver will usually have a better forward current gain than the PNP Darlington.

It does represent a slight compromise in symmetry since the output resistance is higher for the compound-pnp than for the npn Darlington. This option may induce a mild asymmetry in $V_{L(t)}$ depending on load $R_L$. 

![Figure 13.7-4: The VBE multiplier](image)

![Figure 13.7-5: Class-AB Darlington configurations.](image)
Analysis of the VBE multiplier is not much different from the process used for example 13.7-1, except that we now need to identify the appropriate value of $V_{BB}$ in order to find the correct values for $R_1$ and $R_2$.

If the super-beta pairs are deployed as represented by figure 13.7-5a, then $V_{BB} \approx 4 \times 0.6V$.

**EXAMPLE 13.7-2:** Design a class-AB amplifier for a load requirement $P_L = 32W$ and $R_L = 4\Omega$ using [TIP-120](#) and [TIP-125](#) transistors. These are complementary 65W Darlington monolithic transistors with forward current gain $h_{FE} = 1000$ (see data sheets). Choosing $I_R = 0.5mA$ and require $I_{C5}$ to vary by no more than a factor of 5 is a reasonable design assumption. We might assume reference transistor Q5 to be an (unspecified) 5W transistor.

Determine
- (a) $V_S(min)$ and $I_B(max)$
- (b) quiescent current $I_Q$ and quiescent power $P_Q$
- (c) $I_{bias}$, $R_1$ and $R_2$
- (d) Total worst-case power dissipation budget $P_D$ if $V_S = V_S(min)$
- (e) Total worst-case power dissipation budget $P_D$ if $V_S = 20V$

**SOLUTION:**

(a) Power supply rails must be greater than $V_S = V_L(max) = \sqrt{2R_L P_L(max)} = \sqrt{(2 \times 4 \times 32)} = 16.0V$

for which the maximum load current is $I_L(max) = \frac{V_L(max)}{R_L} = \frac{16}{4} = 4.0A$

Since the Darlington pair has equivalent $\beta_F = 1000$ then $I_B(max)$ is approximately

$$I_B(max) \approx \frac{I_L(max)}{\beta_F} = \frac{4.0}{1000} = 4.0mA$$

(b) Assume $I_B(min)$ is negligible $\approx 0$. Since $I_{bias} = I_R + I_B + I_{C5}$ then

$$I_{C5}(max) + I_B(min) = I_{C5}(min) + I_B(max)$$

or $5I_{C5}(min) = I_{C5}(min) + 4mA$, which gives $I_{C5}(min) = 1.0mA$ and therefore

$$I_{C5}(max) = 5.0mA$$

Since Q5 = (5W/65W) = 1/13 the size of Q1, then $I_Q \approx 13 \times I_{C5}(max) = 65mA$.

(c) At quiescent, $V_{BE5} \approx 0.6V$ (default), so $R_I = V_{BE5}/I_R = 0.6V/0.5mA = 1.2k\Omega$. Since the $V_{BE}$ multiplier must bias an equivalent of four junctions, three more $V_J = 0.6V$ must fall across $R_2$ and therefore
\[ R_2 = (3 \times 0.6\text{V})/I_R = 1.8\text{V}/0.5\text{mA} = 3.6\text{k}\Omega \]

\[ I_{bias} = I_R + I_B(\text{min}) + I_C(\text{max}) = 0.5\text{mA} + 0 + 5.0\text{mA} = 5.5\text{mA} \]

\[(d) \text{ For voltage rails } V_S = V_S(\text{min}) = 16.0\text{V}, \quad P_D(\text{worst, class-B}) = 0.406 \times \frac{1}{2} \frac{V_S^2(\text{min})}{R_L} \]
\[ = 0.406 \times (32\text{W}) = 13.0\text{W} \text{ and } P_Q = I_Q \times (2V_S) = 65\text{mA} \times (2 \times 16) = 2.08\text{W} \]

so the total worst-case power dissipation = 13.0W + 2.1W = \textbf{15.1W}

\[(e) \text{ For voltage rails } V_S = 20.0\text{V}, \quad P_D(\text{worst, class-B}) = 0.406 \times \frac{1}{2} \frac{V_S^2}{R_L} \]
\[ = 0.406 \times (0.5 \times 20^2/4) = 20.3\text{W} \text{ and } P_Q = I_Q \times 2V_S = 65\text{mA} \times (2 \times 20) = 2.6\text{W} \]

so the total worst-case power dissipation = 20.3W + 2.6W = \textbf{22.9W}

A larger cooling system penalty must be paid when \(V_S > V_S(\text{min})\) even though no more power is applied to the load than at the ideal (and unrealistic) choice \(V_S = V_L(\text{max})\).

\[ \]

13.8 OTHER AMPLIFIER CONSIDERATIONS

**Instantaneous Power Dissipation**

In the overview so far, it has been have taken for granted that the thermal time constants are much longer than the time constants of the signal. The assessment of power \(P_D\) in the circuit has been able to be defined in terms of time averages. However, nothing prohibits the levels of current and voltage to have an instantaneous level of power consumption that exceeds the \(P_D(\text{max})\) of the power dissipation hyperbolas. The time averaging process may be a bad call if the signal time constant is very low. For example, a linear power amplifier intended to drive a servo motor control may have the operation stop for long periods of time at point A, and \(P_D\) is then defined in terms of the “long” instant. In such an application, the transistor dissipation must be analyzed in terms of a worst-case instantaneous power dissipation scenario. For a linear load line as represented by load resistance \(R_L\), the maximum instantaneous dissipation occurs at the center of the load line, for which

\[ P_D = \frac{V_S}{2R_L} \times \frac{V_S}{2} = \frac{1}{2} \times \frac{V_S^2}{2R_L} = 0.5P_L \]

where sinusoidal signals are still assumed, just at a longer time constant.
Power gain

It is essential and is expected that the power amplifier stage have a high intrinsic power gain. In most cases this is reflected by the caveat of high current gain since the output drivers are of the form of voltage-follower circuits. But the corollary is that the power amplifier must have a high input impedance. This requirement is no problem for the FET amplifiers, assuming that we don’t go too high in frequency. But it presents a little greater problem to BJT drivers, since the input impedance depends on $\beta_F$. The “super-beta” transistors are therefore almost a caveat to this requirement, since that the input impedance of the emitter-follower circuit is approximately

$$R_{in} = (\beta_F + 1)R_L$$

For very high power, high-voltage transistors, even the Darlington configuration has some limitations, particularly for the PNP output transistors for which $\beta_F$ may be as low as 5 to 10. In this respect the compound pnp option may be a caveat of high-power design.

Inductive loads

Many of the high-power applications include inductive loads, particularly those for which an electromechanical device is being controlled. Inductive loads are prone to the creation of large voltage transients at the output node of the transistor when output current changes too rapidly through the inductance. This induced emf is the caveat of the energy stored in an inductance, for which it reflects a transfer of energy into a voltage mode in response current change, as reflected by

$$V = L \frac{dI}{dt}$$

(13.8-1)
This induced emf can be catastrophic to the output transistors of the power amplifier since it can exceed the inverse breakdown voltage of the power transistor. For this reason power amplifiers with inductive loads should be bridged by clamping diodes or snubbers as represented by figure 13.8-2. During normal operation these diodes are reverse-biased. During overvoltages they forward bias and allow the induced emf to harmlessly discharge into the power rails.

**Figure 13.8-2:** Use of protective ‘snubber’ diodes with an inductive load.

**Short-circuit protection and fold-over current limiting**

An accidental short-circuit to ground or an overload at the output, both of which are not uncommon, represents a potentially fatal situation. Assuming that the power supply has a comfortable margin of current that it can provide, the power amplifier will let its drive transistors handle the situation. The drive transistors will comply for only a short interval before the junction exceeds temperature limits and suffers irreversible effects. To prevent these problems, short-circuit protection is usually necessary. The circuit is shown by figure 13.8-3.

**Figure 13.8-3:** Short-circuit protection for class-AB amplifier.
Transistors Q3 and Q4 are normally off at moderate current load levels. They begin to conduct when there is sufficient current through $R_3$ and $R_4$ to produce a threshold of approximately 0.5V, sufficient to steal base current from the power transistors Q1 and Q2 and thereby limiting current to the load. If the output is shorted the load current limit is effectively

$$I_L(\text{max}) = 0.5/R_3 \quad (13.8-2)$$

Since the voltage drop 0.5V is relatively small compared to the output levels, R3 and R4 will have negligible effect. Because Q3 is not across the power rails, the power it must dissipate is negligible and is a base-drive shunt device, not some type of sacrificial transistor.

A somewhat similar problem is the possibility that an accidental short or low impedance path to one of the voltage rails can occur. This situation will have consequences that are as catastrophic as a short to ground if not more so. We can see from the plot given by figure 13.8-4(a) showing the dissipation hyperbolas (for the class-AB) that one of the drive transistors would be well into an overload should $V_O$ be shorted to $+V_S$ or $-V_S$. Setting lower current short-circuit limits is not a good solution since this would seriously restrict the maximum drive capability of the amplifier.

**Figure 13.8-4**: Foldover protection circuit for class-AB amplifier.
Figure 13.8-4(b) shows a modification of the circuit called a *foldover circuit* which gives an effective short-circuit protection through the extra resistance ladder formed by $R_1$ and $R_2$. When we use this arrangement

$$V_{BE3} = (V_L + I_L R_3) \times \frac{R_2}{R_1 + R_2}$$

and since the voltage at $V_{E3} = V_L$, then the voltage across the base-emitter junction of $Q_3$ is then

$$V_{BE3} = V_{E3} = (V_L + I_L R_3) \times \frac{R_2}{R_1 + R_2} - V_L = \frac{(R_1 R_3 I_L - R_1 V_L)}{R_1 + R_2}$$

If we assume a cut-in value $V_{BE3} = 0.5V$ then the limit relationship is

$$I_L = \frac{R_1}{R_2 R_3} V_L + 0.5 \times \left( \frac{R_1 + R_2}{R_2 R_3} \right)$$  \hspace{1cm} (13.8-3)

Note that this is a current-voltage line which varies with respect to $V_O$, and can be used to limit the current without crossing over the $P_D$ hyperbola, as represented by figure 13.8-4(c). Therefore we have gained a wider range of overload protection with minimum compromise of the load-handling capability of the circuit.

### 13.9 POWER OPAMPS

At a higher level of abstraction and simplicity we may take advantage of technology and packaging. As a consequence of integrated circuit evolutions many applications can be covered by an integrated circuit form of power amplifier which we identify as the *power opamp*. The majority of power opamps are constructed with moderate voltage power transistors and therefore do not encounter the difficulties of integrating high voltage processing technology with lower voltage technologies. Power opamps will invariably incorporate such features as short-circuit protection, current boosters, etc, integrated into the IC package. They are optimized for class-AB operation with minimum quiescent power budget and in this respect closely mimics ideal class-B operation. Therefore for designs with power opamps the worst-case maximum power dissipated in the opamp, $P_D(max)$, is identical to that determined in section 20-6, i.e

$$P_D(max, worst) = \frac{4}{\pi^2} \times \frac{1}{2} \frac{V_S^2}{R_L}$$  \hspace{1cm} (13.9-1a)

And if the power supply rails can be chosen such that $V_S = V_L(max)$ this can be simplified to

$$P_D(max, worst) = 0.406 \times P_L(max)$$  \hspace{1cm} (13.9-1b)
The basic usage issues are then the identification of load and cooling system relationships for which it is necessary to define

1. $V_S(\text{min})$
2. thermally de-rated limit $P_D(\text{max})$

For loads requiring greater levels of power than a single opamp can deliver power opamps may be coupled in parallel. Figure 13.9-1 shows two common options. Even though not represented by the figure, it is also necessary that a small equalization resistance, on the order of $0.1\, \Omega$ be placed between each follower output node and the load to handle unequal offsets in the paralleled opamps.

**Figure 13.9-1:** Circuits configurations using stacked power opamps.

Consider the following example:

**EXAMPLE 13.9-1:** A project requires a $P_L(\text{max})$ of 50W to be applied to a $R_L = 4\, \Omega$ load. Monolithic LM-12 power opamps (80W at $T_{J,\text{max}} = 225^\circ\text{C}$) are available.

Assess possible designs by

(a) determining optimum $V_S$ and minimum heat sink resistance needed under the criterion $T_J < 165^\circ\text{C}$ to prolong device lifetime. Assume use of heat sink grease with $\theta_{CS} = 0.2^\circ\text{C}/\text{W}$.

(b) If a set of stacked opamps with Thermalloy 501303B00000G heat sinks ($\theta_{SA} = 12^\circ\text{C}/\text{W}$) are used, what is the minimum number of opamps needed and their case temperature?
**SOLUTION:** (a) For maximum efficiency the power rails need to be

\[ V_S = V_L(max) = \sqrt{2R_L P_L(max)} = \sqrt{(2 \times 4 \times 50)} = 20\text{V} \]

The LM12 is rated for 80W at \( T_J(max) = 225\text{°C} \). So by equation 13.1-3

\[ \theta_{JC} = (225 - 25)/80 = 2.5 \text{ °C/W} \]

Assuming that the monolithic opamps are optimized to nearly ideal class-B design then

\[ P_D(max, worst) = 0.406 \times P_L(max) = 20.3\text{W} \]

for which we need a heat sink of thermal resistance

\[ \theta_{SA} = (T_J - T_A)/P_D - (\theta_{JC} + \theta_{CS}) = (165 - 25)/20.3 - (2.5 + 0.2) = 4.2\text{°C/W} \]

A heat sink with thermal resistance this low would have to be fairly large.

(b) On the more practical side, opamps can be fitted with the suggested heat sink resistance of \( \theta_{SA} = 12 \text{ °C/W} \) and stacked. The maximum power that each such opamp can dissipate (for \( T_J = 165\text{°C} \)) will be

\[ P_D = (T_J - T_A)/(\theta_{JC} + \theta_{CS} + \theta_{SA}) = (165 - 25)/(2.5 + 0.2 + 12) = 9.52\text{W} \]

for which we will need \( N_{OA} = 20.3\text{W} / 9.52\text{W} = 2.13 \) opamps

Since opamps do not exist as fractional quantities, we will need three opamps \( N_{OA} = 3 \).

The case temperature will then be

\[ T_C = T_A + (\theta_{CS} + \theta_{SA}) \times P_D(ea) = 25 + (0.2 + 12) \times \frac{20.3}{3} = 107.6 \text{ °C} \]

(and the junction temperature will be: \( T_J = 124.5 \text{ °C} \))

Power opamps also provide other configurations for delivering power to a load. One of these is of the form of the power bridge shown by figure 13.9-2. This topology makes use of a unity-gain follower and a unity-gain inverter across a bridged load. As shown by the figure the maximum amplitude across the load is \( V_L(max) = 2V_S \). The power rails then need to be

\[ V_S \geq \frac{1}{2} V_L(max) = \frac{1}{2} \sqrt{2R_L P_L(max)} \] (13-9.2)
Figure 13.9-2: The power bridge: (a) the opamp pair (b) output transistor operation.

Figure 13.9-2(b) shows how the output transistors for the two opamps alternately conduct in the bridge configuration. Peak current $I_L(\text{max})$ is defined by the maximum output amplitude $V_L(\text{max})$ and is

$$I_L(\text{max}) = \frac{V_L(\text{max})}{R_L} \quad (13.9-3)$$

The average current over one half-cycle is the same as that for class-B, i.e.

$$I_L(\text{avg, half}) = \frac{1}{\pi} \frac{V_L}{R_L} \quad (13.9-4a)$$

and conduction takes place for both half-cycles so that a factor of 2 results

$$I_L(\text{avg}) = 2 \times \frac{1}{\pi} \frac{V_L}{R_L} \quad (13.9-4b)$$

The power drawn from the supply is then

$$P_S = 2V_s \times I_L(\text{avg}) = \frac{4}{\pi} \frac{V_s V_L}{R_L} \quad (13.9-5)$$

and so the maximum power dissipated in the circuit is then

$$P_D = P_S - P_L = \frac{4V_s V_L}{\pi R_L} - \frac{1}{2} \frac{V_L^2}{R_L} \quad (13.9-6)$$
The maximum power dissipation $P_{D}(\text{max})$ occurs when $\partial P_{D} / \partial V_{L} = 0$, for which

$$V_{L} = \frac{2}{\pi} (2V_{S})$$  \hspace{1cm} (13.9-7)$$

Substituting (13.9-7) into (13.9-6) the maximum power (= worst-case) dissipated in the circuit will be

$$P_{D}(\text{worst}) = \frac{2}{\pi^{2}} \left( \frac{2V_{S}}{R_{L}} \right)^{2} = \frac{4}{\pi^{2}} \left( \frac{1}{2} \frac{(2V_{S})^{2}}{R_{L}} \right)$$  \hspace{1cm} (13.9-8)$$

This result is exactly the same as for ideal class B as should not be unexpected inasmuch as the topology is a class-B topology, just in bridge form.

Note that the power bridge requires only half the supply voltage as that of the voltage-follower stack but twice the current (per opamp). and since $R_{L}$ is deployed as a bridge between the two outputs, neither end of the load can connect to ground, since half of the waveform output will then be shorted.

Reconsider example #13.9-1(a) but using a power bridge and $V_{S} = \pm 12V$

**EXAMPLE 13.9-2:** Let $P_{L} = 50W$ and $R_{L} = 4\Omega$ (same as exercise 13.9-1) and the use of two 12-V power supplies for a $\pm V_{S}$. By equation (13.9-2)

$$V_{S}(\text{min}) = \frac{1}{2} V_{L}(\text{max}) = \frac{1}{2} \sqrt{2R_{L} P_{L}(\text{max})} = 10.0V$$

$V_{S} = 12V$ satisfies this limit. Equation (13.9-8) then yields a worst-case power dissipation in the circuit of

$$P_{D}(\text{worst, B}) = \frac{4}{\pi^{2}} \times \frac{1}{2} \frac{24^{2}}{4} = 29.2W$$

From exercise 13.9-1 the maximum power that each opamp can dissipate = 9.52W. Then

$$N_{OA} = \frac{29.2W}{9.52W} = 3.06 \text{ opamps}$$

Since a power bridge must be symmetric, an even number of opamps is required. So $N_{OA} = 4$

Consequently the power dissipated in each opamp is $P_{D}(\text{worst,B})$ divided by a factor of 4, for which

$$T_{C} = T_{A} + (\theta_{CS} + \theta_{SA}) \times P_{D}(\text{ea}) = 25 + (0.2 + 12) \times \frac{29.2}{4} = 114.1^\circ C$$
We are also allowed to stack opamps in the power bridge configuration but with the caveat that an even number of opamps is necessary.

13.10 CLASS-D AMPLIFIERS

The class-B amplifier could have an efficiency approaching 100% if it is used to handle a full-voltage square-wave rather than a sinusoidal wave. This greater efficiency results because large currents occur when the transistor is put into its most conductive state, for which the device voltage $V_D, V_{DS}$ or $V_{CE}$ is small. Alternatively, when device voltage $V_D$ is large the transistor is in its least conductive state, and therefore device current $I_D$ is small. Since $P_D = I_D \times V_D$ then it is always small since either the current is nearly zero or the voltage is nearly zero during its operational cycle.

The class-D amplifier is a modification of this principle for which the signal is chopped into rail-rail square-wave pulses as a high-frequency switch-mode operation that alternately connects load $R_L$ to the positive and negative supplies. The class-D amplifier therefore has an efficiency approaching 100%. But in order for it to function as a signal amplifier its input must be of PWM (pulse-width-modulated) form as shown. The output is derived by means of a time-averaged form with appropriate filter time constants.

This requires that the class-D amplifier include a pulse-width modulation front end and a filter circuit on the back end. Switching frequency must be considerably higher than the signal frequency in order to avoid aggravations such as distortion, aliasing, and others associated with pulse-modulation schemes. Usually, a CMOS type of output circuit is used, as represented by figure 13.10-1(a) in order to achieve the switching speed necessary.

![Figure 13.10-1: Class-D amplifier using CMOS output drivers.](image)

The PWM system uses a high-speed comparator to generate the switch-level input, comparing signal input $V_i(t)$ to a sawtooth with amplitude $V_p < V_{(max)}$ at switching frequency $f_s$. The output of the
comparator \( V_d \) must be of amplitude at least twice that needed to switch drive transistors M1 and M2 ‘on’ and ‘off’.

A representative modulator design is shown by figure 13.10-2. The modulator itself is switched by a pulse train of frequency \( f_S \), for which switch Q1 has the effect of discharging capacitance \( C \), which is otherwise linearly charged by and current source \( I_o \). The amplitude \( V_P \) of the sawtooth is

\[
V_P = \frac{1}{f_s} \frac{I_{O}}{C}
\]  

(13.10-1)

Assuming that a CMOS output drive is used similar to that of figure 13.10-1, the CMOS input node will be driven by an input PWM pulse \( V_I = 0.5V_A \pm V_M \) which corresponds to \( V_{GS} = \pm V_M \) for each transistor,
since zero signal (corresponding to \( V_I = V_A/2 \) input) corresponds to gate voltage for each transistor being at the voltage rails. The MOSFETs act as switched resistances for which the ‘on’ state then has an approximate conductance

\[
G_{DS} = \frac{I_D}{V_{DS}} \approx 2K(V_M - V_{TH}) \quad (13.10-2)
\]

The output voltage amplitude to the load is then defined by the voltage divider for which

\[
V_L = \left( \frac{R_L}{R_L + 1/G_{DS}} \right) \times V_S \quad (13.10-3a)
\]

and the power delivered to the load, time-averaged for a sinusoidal input signal, will then be

\[
P_L = \frac{1}{2} \frac{V_L^2}{R_L} = \frac{1}{2} \frac{R_L G_{DS}}{1 + R_L G_{DS}} \frac{V_S^2}{R_L} \quad (13.10-3b)
\]

The current drawn by the transistor and the load is of the form

\[
I_L = \frac{V_L}{R_L} = \left( \frac{G_{DS}}{1 + G_{DS} R_L} \right) \times V_S \quad (13.10-4a)
\]

so that the power drawn from the supply will be

\[
P_S = \left( I_L^2 \right) \times \left( R_L + 1/G_{DS} \right) = \frac{1}{2} \frac{V_S^2 G_{DS}}{1 + G_{DS} R_L} \quad (13.10-4b)
\]

Therefore the efficiency of the amplifier is

\[
\eta = \frac{P_L}{P_S} = \frac{G_{DS} R_L}{1 + G_{DS} R_L} \quad (13.10-5)
\]

This equation, along with 13.10-2, also defines the lower limit of the input amplitude \( V_{M} \). Example 13.10-1 illustrates this analysis.

**EXAMPLE 13.10-1:** A class-D amplifier of the form shown by figure 13.10-1 uses a complementary matched pair of MOSFETs for which \( K = 0.4A/V^2 \) and \( |V_{TH}| = 3.2 \text{ V} \). It is used to provide a maximum of 60W of power to a \( R_L = 5 \text{ } \Omega \) load. Determine power supply requirements \( V_S \) and \( I_S \), and minimum input drive level \( V_{M} \) for operation at 80% efficiency.
SOLUTION: The maximum output voltage level $V_o = V_S$ is given by

$$V_S = \sqrt{2 R_L P_L (\text{max})} = \sqrt{(2 \times 5 \times 60)} = 24.5 \text{V}$$

for which $I_S = V_S / R_L = 4.9 \text{A}$

For an efficiency of 80%, we have, from equation (13.10-5)

$$G_{DS} R_L = \frac{\eta}{1 - \eta} = \frac{0.8}{0.2} = 4$$

for which $G_{DS} = 4 / R_L = 0.8 \Omega$

From equation (13.10-2) we get

$$V_M = V_{TH} + G_{DS} / 2 K = 3.2 + 0.8 / (2 \times 0.4) = 4.2 \text{V}$$
PORTFOLIO and SUMMARY

Thermal:

\[ T_J - T_A = \theta_{JA} P_D \]
\[ \theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \]
\[ \theta_{JC} = \left( T_J (\text{max}) - 25 \right) / P_D (\text{rated}) \]

Power flow:
\[ P_s = P_L + P_D \quad \eta = P_L / P_S \]
\[ \langle P_L (t) \rangle = \frac{1}{2} \frac{V_s^2}{R_L} \]
\[ \langle P_S \rangle = 2 V_s \times \langle I \rangle \]

Class-B/class-AB topology:

\[ V_s (\text{opt}) = V_L (\text{max}) = \sqrt{2 R_L P_L (\text{max})} \]

Class-B:
\[ I_s = \frac{1}{\pi} \frac{V_L (\text{max})}{R_L} \]
\[ V_L (\text{worst}) = V_{LWC} = \frac{2}{\pi} V_S \]
\[ P_d (\text{worst}) = \frac{1}{2} \frac{V_{LWC}^2}{R_L} \approx 0.4 \times \frac{1}{2} \frac{V_S^2}{R_L} \]

Class-AB:
\[ P_{DQ} = 2 V_S I_Q \]
where \[ I_Q = N \times [I_D (\text{max}) / \text{or} / I_{C5} (\text{max})] \]

for thermal analysis: \[ P_D = P_{D \text{(class-B, worst)}} + P_{DQ} \]

= power dissipated in the transistor pair

Opamp (optimized as ~ class-B) (power bridge topology)

\[ V_s (\text{optimum}) = \frac{1}{2} \sqrt{2 R_L P_L (\text{max})} \]
\[ V_L (\text{worst}) = \frac{2}{\pi} (2 V_S) \]
\[ \langle I_s \rangle = \frac{2 V_L (\text{max})}{\pi R_L} \]
\[ N_{OA} = \text{Integer} \left[ P_D (\text{total}) / P_D (\text{ea}) \right] \]
Additional breakout on class-AB topologies

Class AB

\[ V_L(\text{max}) = \sqrt{2 R_L P_L(\text{max})} \]

\[ R_L(\text{min}) = \frac{V_S^2}{2 P_L(\text{max})} \]

\[ \beta_S = \beta_1 \beta_3 + (\beta_1 + \beta_3) \quad \text{Darlington} \]

\[ \beta_S = (\beta_3 + 1) \beta_1 \quad \text{Szklarski} \]

\[ P_D(\text{worst}) = P_{DB}(\text{worst}) + P_{DG} \]

\[ P_{DB}(\text{worst}) = \frac{4}{\pi^2} \frac{V_S^2}{2 R_L} \]

\[ P_{DG} = 2 V_S \times I_Q \]

\[ I_Q = N Q_1 Q_5 \times I_{CS}(\text{max}) \]

\[ I_{\text{bias}} = I_R + I_{CS} + I_{B3} \]

\[ I_{B3}(\text{max}) = \frac{1}{\beta_S} \frac{V_S(\text{max})}{R_L} \]

\[ R_1 = \frac{V_{BE}}{I_R} \approx 0.6 / I_R \]

\[ R_2 = [n(V_T) - 1] \times R_1 \]

\[ P_S = 2 V_S \times \langle I_Q \rangle + P_{DG} \]
Simulation analysis of class-C amplifier

Class-C stage, resonant circuit tuned to carrier input at $f_s = 1.0$MHz.

Output results for signal $V(V_L)$ at the load and $I_C(t)$ passed by the transistor. For $Q = 8$

Using the macros indicated

\[
S(ABS(IC(Q1)*V(Vc)))/\text{Time} = 15.47\text{mW} \quad \text{at} \quad t = 200\text{us} = P_D
\]

\[
S(ABS(-I(R3)*V(VL)))/\text{Time} = 103.3\text{mW} \quad \text{at} \quad t = 200\text{us} = P_L
\]

Gives efficiency $\eta = (103.3)/(15.5 + 103.3) = 87\%$ for $Q = 8$