CHAPTER 2. BASIC CONCEPTS AND RULES OF ENGAGEMENT

2.1 CONDUCTANCE and RESISTANCE

Although it may have seemed preposterous to earlier civilizations that anything could flow through a solid rod of metal, it probably would have had more meaning if they touched the rod to something electrically hot. The concept of there being electrical charge stored at a high potential energy may have been something of a shock to your ancestors, but is now accepted as a natural fact. And the concept of charge flow is also accepted and formulated by the rule known as Ohm’s law.

Ohm’s law is a law of fluid flow. It says that under a pressure difference across a conduit containing charge, charge will flow. The flow rate of the charge will be proportional to the pressure difference (voltage difference) between the ends of the conduit. This concept is mostly just common sense, but is stated as

\[ I = GV \]  \hspace{1cm} (2.1-1a)

where \( I \) is the charge flow in Coul/sec, \( V \) is the voltage (electrical pressure difference) in Volts and \( G \) is the conductance of the conduit. Ohm’s law is also stated as

\[ V = IR \]  \hspace{1cm} (2.1-1b)

Where \( R = I/G \) is defined as the resistance. The usage of \( I \) for electrical current, \( V \) for voltage, \( G \) for conductance and \( R \) for resistance is the conventional electrical nomenclature.

The distinction of an electronic fluid is that it is a flow of charges (quantized by \( q = 1.6 \times 10^{-19} \text{C} = \text{single electron charge} \)). It is also called an electron gas since it can be compressed, although we will not do so until later.

Some conduits are more conductive to the flow of electrical charge than are others. The conductance depends on (1) geometry and (2) conductive properties of the material (otherwise known as conductivity). The reality of the property of conduction is that all materials will conduct electrons, some more than others. Metals are very conductive. Oxides are not. Electrical conduction properties are typically identified by tables, either of conductivities or of resistivities.

Figure 2.1 shows a representation of a uniform geometry for a conductance (or resistance) with cross-section of area \( A \) and length \( L \). Within an electronic circuit, strips of material not unlike that of the geometry shown form the conductive paths for flow paths of the electronic fluid.
Figure 2.1-1. Representation of electrical conductance/resistance (uniform geometry)

The figure tells all. The conductance is

\[ G = \sigma \frac{A}{L} \]  \hspace{1cm} (2.1-2a)

and/or the resistance is

\[ R = \rho \frac{L}{A} \]  \hspace{1cm} (2.1-2b)

The coefficients \( \sigma \) and \( \rho \) are the conductivity and resistivity, respectively. These symbols are the ones used in the table referenced by the URL and are the conventional notation.

From the point of view of a flow of charge fluid it should make sense that a conduit with more cross-sectional area \( A \) will proportionally allow more current to flow. If \( A_2 \) is twice as large as \( A_1 \) then twice as much fluid will flow. And a conductance with twice the length \( L \) would be half as conductive. Equations (2.1-2a) and (2.12b) are statements thereto.

In circuit context the conductance path is more likely formulated in terms of its resistance to the flow of current. Resistance carries the unit of choice. The measure is in the ohm (symbol: \( \Omega \)) and is defined by Ohm’s law as (1\( \Omega \) = 1 Volt/Amp). So the coefficient of resistivity (= \( \rho \)) must then be in terms of (\( \Omega \).m) (in semiconductor context it is more often given in \( \Omega \).cm). Conductivity is given in terms of (1/\( \Omega \).m) or more correctly, as Siemans/meter (S/m). With equations (2.1-2a) and (2.1-2b) that confirms resistance in \( \Omega \) and conductance in mho (= ohm spelled backwards) (symbol: \( \mathbb{U} \)). The \( \mathbb{U} \) symbol is difficult to find in print but is more commonly used for conductance measure than is Siemans.

Since many orders of magnitude are possible, prefixes are common and should be used with relative fluency and abandon. Later in the practice of semiconductor electronics the resistances will likely default to k\( \Omega \) and current to mA. This is sometimes called the k\( \Omega \) – mA convention since milliamperes (mA) result when potentials in volts are applied across k\( \Omega \).

Consider the following example
EXAMPLE 2.1-1(a): An integrated circuit interconnect strip of polysilicon is printed on an insulated substrate. What is its resistance?

SOLUTION: From equation (2.1-2b) the mathematics is

\[ R = \rho \times \frac{L}{A} = 0.25 \, \text{cm} \times \frac{20 \, \mu m}{2.0 \, \mu m \times 1.0 \, \mu m} = 0.25 \times \frac{20}{2.0 \times 1.0} \times 10^4 = 2.5 \, \text{k}\Omega \]

Even though this mathematics is complete and sufficient it has some extra overhead in the prefixes. Note the factor of $10^4$. It is the units conversion from cm to $\mu$m. The relative relationships for unit prefixes are an essential part of your knowledge base. Pausing over conversion details is only for the unpracticed.

Also notice that the answer was not in $\Omega$ but in $\text{k}\Omega$. The result must be in a sensible form. Scientific notation is not invalid but is not used when dealing resistance measure.

EXAMPLE 2.1-1(b): It appears that the stripe of example 2.1-1(a) is actually two strips in parallel. What is the resistance of one of these strips?

SOLUTION: From equation (2.1-2b) the mathematics is

\[ R = \rho \times \frac{L}{A} = 0.25 \, \text{cm} \times \frac{20 \, \mu m}{1.0 \, \mu m \times 1.0 \, \mu m} = 0.25 \times \frac{20}{1.0 \times 1.0} \times 10^4 = 5 \, \text{k}\Omega \]

This was an unnecessary calculation. It should be fairly evident that a single stripe is half as conductive as two in parallel. And if the conductance is half then the resistance is twice.
These two examples point out a context fact that should be added to your knowledge base as a simple rule of resistance topologies, namely that conductances in parallel will add, i.e.

\[ G_{eq} = G_1 + G_2 + G_3 \quad (2.1-3a) \]

Which is the same as

\[ \frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \quad (2.1-3b) \]

The rule is stated in terms of resistances since resistance are the circuit component, usually given in terms of ohms (or k\(\Omega\)). Consider the exercise set of Example 2.1-2.

**EXAMPLE 2.1-2** What is the equivalent resistance of each of the parallel resistance options shown?

**SOLUTIONS** By inspection, listed in parentheses.

The symbol for resistance (shown) looks like a crinkled channel even though it most likely is a thin film or a surface strip. Carbon films are a favored choice for discrete resistance components.

The absence of math calculations in Example 2.1-2 reflects the suggestion that simple topologies should be done by inspection, even if approximate (as was done for parts (d), (e) and (f) of the above example).

Example 2.1-2 represents the ‘old school’ form, as if a circuit were assembled from discrete parts. But reality is that circuits are now more likely to begin their existence as a printed form for which resistances are either connection paths or designated stripes.

The simplicity of calculation is even more evident for resistances in series. Consider Example 2.1-1(b) if the length is assessed as a sum of sections.
**EXAMPLE 2.1-3:** What are the resistances of the two segments? Assume polysilicon.

<table>
<thead>
<tr>
<th>Material</th>
<th>Resistivity (Ω·cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>$2.7 \times 10^6$</td>
</tr>
<tr>
<td>Cu</td>
<td>$1.7 \times 10^6$</td>
</tr>
<tr>
<td>Si (pure)</td>
<td>$3.2 \times 10^7$</td>
</tr>
<tr>
<td>Si (normal doping)</td>
<td>0.25</td>
</tr>
</tbody>
</table>

**SOLUTION:**

\[
R_1 = \rho \times \frac{L_1}{A} = 0.025 \, \Omega \cdot cm \times \frac{8 \mu m}{1.0 \mu m \times 1.0 \mu m} = 0.025 \times \frac{8}{1.0 \times 1.0} \times 10^4 = 2.0k\Omega
\]

\[
R_2 = \rho \times \frac{L_2}{A} = 0.025 \, \Omega \cdot cm \times \frac{12 \mu m}{1.0 \mu m \times 1.0 \mu m} = 0.025 \times \frac{12}{1.0 \times 1.0} \times 10^4 = 3.0k\Omega
\]

This was another example of doing more math than necessary. It should be evident that a strip of 8μm length is (= 2/5) times that of a 20μm length. Then \(R_1 = (2/5) \times 5.0k\Omega = 2.0k\Omega\), by inspection.

Using the answer from Example 2.1-2(b) \(R_{eq} = 5k\Omega = 2k\Omega + 3k\Omega\).

Example 2.1-3 emphasizes the rule of resistances in series which is

\[
R_{eq} = R_1 + R_2 + R_3
\]

(2.1-4)

**EXAMPLE 2.1-3:** What is the equivalent resistance of each of the resistance topologies shown?

**SOLUTIONS:** By inspection, answers listed in parentheses.
As reflected by the example it is worth noting that the subsets of resistances, whether series or parallel, can be done by inspection. In these examples the numbers are designed for simplicity. But even if they were not, a fairly reasonable result can still be roughed out. For example part (b) should acknowledge that $3k\Omega || 6k\Omega = 2k\Omega$ by inspection. And then $R_{eq}$ will be $2k\Omega + 2k\Omega = 4k\Omega$.

Similar situations exist with the other topologies. For example the right end of part (e) has $24k\Omega || 8k\Omega = 6k\Omega$ by inspection. And from there $6k\Omega + 6k\Omega = 12k\Omega$, which is in parallel with $6k\Omega$, which gives $4k\Omega$ by inspection. The $4k\Omega$ is in series with $8k\Omega$ and that is in parallel with the $12k\Omega$ at the front end to give an $R_{eq}$ of $6k\Omega$. All is done by inspection. A symbolic representation of the decomposition process for part (e) is shown by figure 2.1-2.

**Part (f) of Example 2.1-3 is a special topology known as a binary ladder, also called an $R$-$2R$ ladder.** The result $R_{eq} = 2R$ is derived by a right-to-left, step by step process like that of figure 2.1-2 and is the outcome no matter how long the ladder may be. The $R$-$2R$ ladder should be consigned to your special circuits collection since it has considerable utility.

The rest of the story is that the resistance topologies serve to sort and divide electrical current and voltage according to Ohm’s law. The topology therefore begins to take the form of a network, consisting of components in the form of branch elements and junctions between components in the form of nodes.

The simplest of the passive components are resistances, but as the reach of circuit topologies is extended, some of the branches will be sources and others will be various forms of control and reactive elements.

Since a network will distribute electrical quantities along and through the network of nodes and branches it is in order that sources of electromotive energy be included in the mix. The simplest source is that of the electrochemical cell, a.k.a. ‘battery’ and the symbol (two equivalent forms) is shown by Figure 2.1-3. The figure also shows a common usage of resistances in series with a voltage source and serves to form a particularly useful topology called a voltage divider.
Voltage dividers are a means of parsing the source voltage into lesser fractions. This context also gives rise to a special slide-wire resistance component called a potentiometer, represented by figure 2.1-4. The potentiometer has a wiper arm that rides upon a track. Many circuits that have a fine-tuning requirement may include one or more ‘pots’ with a screw slot. Precision circuit applications often include a potentiometer with a helical slide track.

2.2 NODE VOLTAGES and BRANCH CURRENTS

As represented by the resistance ladders, a circuit is a set of paths and junctions. It may be extended in all directions and be interconnected as an array of branches and nodes. The lace of interconnections is assumed to be ideal with zero resistance (unless the interconnect material happens to be a poor conductor as in the case of refractory metals). As a mathematical necessity all circuit topologies should have a reference node, usually identified as ‘ground.’ Circuit simulation software always requires a ground node. All of the other node voltages may then be identified relative to the ground (GND) reference.

The ground symbol sneaked into the discussion on voltage dividers because they were an application oriented toward voltages. Relative to the reference point (i.e. GND) the network will be characterized by a set of node voltages (all relative to GND) and a set of branch currents. And even though we may not
necessarily need to know each and every one of the electrical facts of the network, the rest of the story is in the analysis methods by which the circuit can be decomposed and its electrical facts identified.

If the topology is a ladder of series and parallel resistance combinations, its electrical facts can be decomposed in the same way the resistance network was decomposed, but also by use of the rules of voltage division represented by equation (2.2-1).

\[ V_B = \frac{R_2}{R_1 + R_2} \times V_A \]  

(2.2-1)

for which \( V_A \) is the voltage value of a parent node (as illustrated by the figure) relative to ground and the outcome \( V_B \) is also relative to ground.

Decomposition of the node voltages for a ladder network is illustrated by figure 2.2-1. Figure 2.2-1 is the same as that of figure 2.1-2 except that a GND and a source voltage are included. Consequently the node voltages can be extracted by voltage division from left to right. Branch currents can subsequently be obtained from the node voltages and resistances if desired.

\[
\begin{align*}
V_A &= V_S = 24\text{V} \\
V_B &= \frac{4}{8 + 4} \times V_A = \frac{4}{12} \times 24 = 8.0\text{V} \\
V_C &= \frac{6}{6 + 6} \times V_B = \frac{6}{12} \times 8 = 4.0\text{V} = V_s \\
I_s &= \frac{V_s}{8} = \frac{4.0}{8} = 0.5\text{mA} \\
I_S &= \frac{V_S}{R_{eq}} = \frac{24}{6} = 4.0\text{mA}
\end{align*}
\]

Ladder topologies of the form represented by figure 2.2-1 are primarily concept exercises. In contrast, the R-2R ladder is of functional significance since no matter how many stages it may have \( R_{eq} = 2R \). And
therefore each stage will consist of an $R$ in series with a next stage $R_{next} = R$, which then forms a divide-by-two voltage divider as illustrated by figure 2.2-2.

Figure 2.2-2. R-2R ladder. Decomposition = divide-by-2 for each stage. $V_N = V_S/2^N$

Since each stage is a divide-by-2 then the node voltages along the ladder may be ascertained by a divide-by-two count from the source node, as shown by the figure. And since the node voltages are a divide-by-two, the branch currents are also a divide-by-two. As well as being electrically simple and direct it should be evident why the R-2R ladder belongs in the special collection of circuit toplogies.

Most circuit topologies do not decompose as readily as do the ladder forms. So general rules associated with the nodes and branches of the network are of necessity. There are two rules for networks, identified in 1845 by a gentleman named Gustav Kirchoff, and known as Kirchoff’s laws. The first is a law of nodes and is given by

$$\sum_{node} I_K = 0 \quad (2.2-2)$$

It is a law of conservation of current. Equation (2.2-2) is called Kirchoff’s current law (KCL). In effect the statement is that ‘current out = current in’. By convention the current out of a node is designated as positive and the current into the node is designated as negative. Sometimes direction may be indicated by an arrow, in which case the polarity of the discovered value will determine whether the arrow was a good choice of flow direction.

The second of the Kirchoff laws is a statement about the potential drops around a loop, and is given by

$$\sum_{loop} V_K = 0 \quad (2.2-3)$$

Equation (2.2-3) is called Kirchoff’s voltage law (KVL) and recognizes that the sum of voltage increments and decrements around a loop must add to zero. It is an electrical statement of the conservation of potential energy. Around a loop the circuitous return to its starting place will bring the
potential energy back to its starting potential. The convention is that the CW (clockwise) direction around a node will be positive and that resistance branch components will each have a positive voltage ‘drop’ across them due to Ohm’s law as stated by equation (2.1-1b).

These two network laws offer a simple and straightforward means for decomposition of the network into electrical facts. For the simplest case in which the branches are of the form of resistances, Ohm’s law equations (2.1-1a) and (2.1-1b) produce a set of (linear) equations amenable to linear computational algorithms. And whether the process is done by back-of-the-envelope or by simulation software, node voltages and branch currents (a.k.a the electrical facts of the topology) can be efficiently resolved.

All of the electrical facts within a network are a consequence of the energy sources embedded within the network structure. Courtesy of the two forms for electrical energy, electrical sources will fall into two possibilities: (1) voltage sources and (2) current sources. The ideal forms and symbols of these source options are represented by figure 2.2-3, along with their electrical characteristics.

Source characteristics are not just defined by the level of electrical energy but also by the slopes of their electrical (I vs V) specifications. In figure (a) the slope of infinity corresponds to a slope conductance of infinity. Therefore an ideal voltage sources will have zero resistance and can provide any level of current at the voltage specified, whether to warm up a resistance or to displace a small planet. A slope of zero is a conductance of zero and so ideal current sources have infinite resistance and provide any level of voltage at the current specified, no matter what magnitude or polarity. Ideal sources are of computational simplicity but are also a little excessive since they can promise anything, no matter how unrealistic.

Current sources may sound like an artifact but there is a component (discussed later) which will act very much like an ideal current source.

The identification of the current source as an energy source also lends itself to identification of another simple and direct topology, called a current divider, shown by figure 2.2-4.
Figure 2.2-4. Current divider. For part (b) $I_1 = 1.0\text{mA}$, $I_2 = 1.5\text{mA}$ and $I_3 = 0.5\text{mA}$

Current division results for path resistances in parallel. Parallel paths parse the available current according to their conductances, i.e.

$$I_3 = \frac{G_3}{G_2 + G_3} \times I_1 \quad (2.2-4)$$

where $I_1$ is the value of the current of parent branch. Equation (2.2-4) might be compared to that of the voltage divider (equation (2.2-1)). The current divider is a common subcircuit topology.

Whatever the form in which electrical energy may exist, the circuit will have the effect of parsing it into sums and fractions. So the rest of the story is in the network topology. Small subsets in the form of parallel and series combinations can be subdued and asserted as simplifications. But in most part the network will need to be resolved by KCL and KVL.

The more general analysis acknowledges a circuit topology as a network of interconnected active and passive branches. As a first cut it will suffice to let the passive branches be of the form of resistances until more entertaining components are addressed. ‘Nodes’ are not unlike solder junctions even though the solder blob analogy suffers if the circuit is an integrated circuit rather than a joined assembly. Nodes may be stretched or spread, but in most part will be an identifiable junction point.

A node will selectively link to other nodes by its set of connecting branches. Then KCL and Ohm’s law equation (2.1-1a) $I = GV$ will give a sum of conducting links from any one node to the other nodes at the ends of its set of branches. There will be as many equations as there are nodes. The result is a set of simultaneous equations of the form:

$$G_{i1}V_1 + G_{i2}V_2 + \cdots + G_{in}V_n = I_{s1}$$
$$G_{s1}V_1 + G_{s2}V_2 + \cdots + G_{sn}V_n = I_{s2}$$
$$\vdots$$
$$G_{s1}V_1 + G_{s2}V_2 + \cdots + G_{sn}V_n = I_{sn} \quad (2.2-5)$$

where the $G_{ij}$ are sums of conductances. Since a node is not usually connected to each and every one of the other nodes many of the $G_{ij}$ terms will be zero (a.k.a. sparse). This method is called nodal analysis.
Consider the network of figure 2.2-5, which is chosen because it contains both types of sources and a tractable set of resistance branches.

The convention is that positive flow is out of the node. Then nodal analysis at node $V_C$ will be

$$-I_S + \frac{(V_C - V_A)}{R_4} + \frac{(V_C - V_B)}{R_3} = 0 \quad (2.2-5)$$

If this is reorganized into an equation in nodal form then

$$\begin{bmatrix} 1 & 1 \\ R_3 & R_4 \end{bmatrix} \begin{bmatrix} V_C \\ V_B \end{bmatrix} - \begin{bmatrix} 1 \\ R_1 \end{bmatrix} V_A - \begin{bmatrix} 1 \\ R_4 \end{bmatrix} V_A = I_S \quad (2.2-6)$$

The form of equation (2.2-6) is less clumsy if we use conductances instead of resistances, i.e.

$$(G_3 + G_4) V_C - G_3 V_B - G_4 V_A = I_S \quad (2.2-7)$$

As a shortcut, use the concept that each node voltage will ‘push’ a (+) current out to the other nodes and the other nodes will ‘push back’(-). If we apply this principle to node $V_B$ then

$$(G_1 + G_2 + G_3) V_B - G_3 V_A - G_4 V_A = 0 \quad (2.2-8)$$

Equation (2.2-8) avoids the extra steps used to acquire equation (2.2-7). Take note that the GND node cannot ‘push back’ since it has value zero.

And (for this example) node $V_A$ needs no equation since it is constrained to be the same as the source $V_S$.

So we might let values be added to figure 2.2-5. The network of figure 2.2-5 with values is represented by example 2.2-1.
EXAMPLE 2.2-1: For the network shown execute a nodal analysis to determine node voltages and branch currents.

SOLUTION: (1) Node \( V_A = 5.0 \) (= constraint)

(2) Node \( V_B \) (using equation (2.2-8) gives

\[
(0.5 + 1.0 + 2.0)V_B - 1.0 \times V_C - 0.5 \times 5.0 = 0
\]

(3) Node \( V_C \) gives

\[
-1.0 \times V_B + (1.0 + 1.0)V_B - 1 \times 5.0 = 2.0
\]

So we are left with

\[
3.5V_B - V_C = 2.5
\]

\[
- V_B + 2V_C = 7.0
\]

eliminating \( V_C \) (Gaussian elimination: multiply top equation \( \times 2 \) and add to the bottom equation) gives

\[
(7.0 - 1)V_B = (5 + 12) \quad \text{or} \quad V_B = 2.0V
\]

Back substitution of \( V_B = 2.0 \) into the first equation gives \( V_C = 4.5V \)

Knowledge of all of the node voltages gives

\[
I_1 = (5 - 2)/2.0 = 1.5mA
\]

\[
I_2 = (2 - 0)/0.5 = 4.0mA
\]

\[
I_3 = (2 - 4.5)/1.0 = -2.5mA
\]

\[
I_4 = (5 - 4.5)/1.0 = 0.5mA
\]

Be aware that it would have been much simpler to let pspice do the grit and grind of the numerical work (as shown).

Nodal analysis is usually the simplest and most direct method by which the electrical facts of a network may be ascertained and is the method favored by circuit simulation utilities.

The other network analysis method makes use of KVL and equation (2.1-1b) and is based on circuit loops. As a convention the set of loops are interior loops, although that is not a hard and fast requirement. The loop mathematics is defined by a set of unknown loop currents with conceptual flow direction being clockwise. So the application of KVL will give a set of simultaneous equations of the form
where the $R_{jk}$ are sums of resistances and the $I_j$ are the loop currents. Loop analysis also goes by the name mesh analysis and each loop is defined by a loop current. The solution of equation (2.2-9) gives the loop currents and then the currents in the various branches of the circuit are then determined from the loop currents. The default flow direction of a loop current is clockwise.

The concepts are represented by figure 2.2-6 which is a 3-loop topology.

Applying KVL to loop $I_A$ of figure 2.2-6b and an $I \times R$ drop across each resistance gives

$$-V_B + (I_A - I_B) R_1 + (I_A - I_C) R_1 = 0 \quad (2.2-10)$$

Take note that voltage drops across resistances that are shared with an adjacent loop will link $I_A$ to neighbor loop currents. If this equation is reorganized to a more convenient form then

$$(R_1 + R_2) I_A - R_1 I_B - R_3 I_C = V_S \quad (2.2-11)$$

As a shortcut it we might note that the terms associated with the $I_A$ loop are positive and the contribution by those for the adjacent loops are negative. Then by inspection, loop $I_B$ will be

$$-R_1 I_A + (R_1 + R_4 + R_3) - R_3 I_C = 0 \quad (2.2-12)$$

The current in loop $I_C$ is defined by the current source $I_S$ so that $I_C$ is constrained to be

$$I_C = -I_S \quad (2.2-13)$$
EXAMPLE 2.2-2: For the network shown execute a loop analysis to determine branch currents and node voltages.

**SOLUTION:**

1. Loop current $I_C = -2\text{mA}$ (constraint)

2. Loop $I_A$ (using equation (2.2-11)) gives

   $$ (2.0 + 0.5)I_A - 2.0 \times I_B - 0.5 \times (-2) = 5 $$

3. Loop $I_B$ gives

   $$ -2.0 \times I_A + (2.0 + 1.0 + 1.0) \times I_B - 1.0 \times (-2) = 0 $$

So we are left with

- $2.5I_A - 2I_B = 4$
- $-2I_A + 4I_B = -2$

eliminating $I_B$ (Gaussian elimination: multiply top equation $\times 2$ and add to the bottom equation):

$$ (5.0 - 2) I_A = (8 - 2) \rightarrow I_A = 2.0\text{mA} $$

And back substitution of $I_A = 2\text{mA}$ in the second equation gives $I_B = +0.5\text{mA}$

Knowledge of the loop currents gives the branch currents

- $I_1 = (I_A - I_B) = (2 - 0.5) = 1.5\text{mA}$
- $I_2 = (I_A - I_C) = (2 - (-2)) = 4.0\text{mA}$
- $I_3 = (I_B - I_C) = (0.5 - (-2)) = 2.5\text{mA}$
- $I_4 = I_B = 0.5\text{mA}$

Node voltages are $V_A = V_S = 5.0\text{V}$ (by constraint)

- $V_B = 0.5 \times I_2 = 0.5 \times 4.0 = 2.0\text{V}$
- $V_C = V_A - I_4 \times R_4 = 5 - 0.5 \times 1.0 = 4.5\text{V}$

and the answers are the same as Example 2.2-1. Once again we might acknowledge that it would have been much simpler to let pspice do the grit and grind numerical work as shown.

As illustrated by the two examples it should be evident that the nodal analysis (KCL) method and the loop analysis (KVL) method are equals in the world of circuit analysis. Simulation software prefers nodal
analysis since the node count defines the number of simultaneous equations and the size of the conductance matrix as represented by the linear equation form

$$\begin{bmatrix} G_{11} & \cdots & G_{1n} \\ \vdots & \ddots & \vdots \\ G_{n1} & \cdots & G_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} = \begin{bmatrix} I_{S1} \\ \vdots \\ I_{Sn} \end{bmatrix}$$

(2.2-14)

where $G_{jk}$ are conductance sums. The diagonal terms will always be sums of positives and the off-diagonal terms will always be sums of negatives. Source terms $I_{Sk}$ should be expected to be relatively sparse as reflected by example 2.2-1. Off-diagonal $G_{jk}$ should also be relatively sparse.

Likewise the mesh analysis will be a linear set of equations of the form

$$\begin{bmatrix} R_{11} & \cdots & R_{1n} \\ \vdots & \ddots & \vdots \\ R_{n1} & \cdots & R_{nn} \end{bmatrix} \begin{bmatrix} I_1 \\ \vdots \\ I_n \end{bmatrix} = \begin{bmatrix} V_{S1} \\ \vdots \\ V_{Sn} \end{bmatrix}$$

(2.2-15)

where $R_{jk}$ are resistance sums. The diagonal terms will be sums of positives and those that are off-diagonal will be sums of negatives. The source terms $V_{Sk}$ should be expected to be relatively sparse and off-diagonal $R_{jk}$ terms are usually also sparse.

Mesh analysis may have difficulty in selection of the best set of interior loops since the circuit simulation software is blind. It also may have difficulty if the network is not planar.

The primary application for the general KCL and KVL nodal and mesh methods is in circuit simulation platforms since linear algebra is a quick and simple inversion. Otherwise these methods afford a general means to the user to derive predictive algebraic forms if the topology is fortunate enough to be relatively small and self-contained.

### 2.3 THEVENIN and NORTON EQUIVALENT CIRCUIT THEOREMS and MAXIMUM POWER THEOREM

Electrical networks are always a part of system and consequently will be vested with one or more I/O ports. The most basic black-box formulation will be that of the two-port network, with an input port and an output port. Multi-terminal ports are diagnosed as a superset of two-terminal ports.

And key to the network function is the output port. It has two terminals one of which is GND. The port therefore will appear to be a source limited by an internal resistance, not unlike that of non-ideal voltage source. As an equivalent voltage source its internal resistance is the factor that limits the current. This perspective and reduced equivalent network is known as Thevenin’s theorem. The output port is otherwise expected to drive an external load $R_L$. The Thevenin theorem is represented by figure 2.3-1.
Figure 2.3-1(a) represents a circuit which otherwise is a mix of active branches and passive branches. Figure 2.3-1(b) represents its Thevenin equivalent, which is a voltage source $V_{th}$ and a limiting resistance $R_{th}$, also called the Thevenin voltage and the Thevenin resistance, respectively.

![Thevenin theorem representation](image)

**Figure 2.3-1.** Thevenin theorem representation. Figure (a) is the (representative) network and Figure (b) is the Thevenin equivalent.

A dual form of Thevenin’s theorem is shown by figure 2.3-2 and is called Norton’s theorem which restates Thevenin’s theorem in terms of an equivalent current source $I_n$ shunted by resistance $R_n$.

![Norton’s theorem representation](image)

**Figure 2.3-2.** Representation of Norton’s theorem. Figure (a) is the (representative) network and Figure (b) is the Norton equivalent.

Since the two interpretations must have the same electrical effect then

\[
I_n = V_{th} / R_{th} \tag{2.3-1a}
\]

\[
V_{th} = I_n R_n \tag{2.3-1b}
\]

\[
R_n = R_{th} \tag{2.3-1c}
\]

and sometimes it is convenient to recognize this equivalence of the two interpretations by the schematic equivalent representation as shown by figure 2.3-3.
Figure 2.3-3. Source equivalence: The two circuit forms are equivalent and are the schematic representation of equations (2.3-1a), (2.3-1b) and (2.3-1c).

The realization of Thevenin equivalent circuits is readily achieved courtesy of the reduction methods and network analysis techniques used heretofore. When there is no load, $V_{th}$ is merely the value of the node voltage at the output node. And when all of the electromotive sources are turned off, then there is nothing left but the resistance network, which can be collapsed to a single $R_{th}$ ($= R_n$) value. Thevenin resistance $R_{th}$ is also the output resistance and may also be acknowledged as $R_{out}$.

Electromotive forces may be due to sources of different types. A voltage source with $V_S = 0$ is a short circuit since an ideal voltage source has zero resistance. A current source with $I_S = 0$ is an open circuit since an ideal current source has infinite resistance. When these criteria are applied to the Thevenin and Norton source equivalents of figure 2.3-3 then the resistance ‘into’ the output port = $R_{th} = R_n$ ($= R_{out}$).

Consider the following example (Example 2.3-1)

**EXAMPLE 2.3-1:** Determine the Thevenin equivalent resistance $R_{th}$ for the circuit of Example 2.2.1 if output is at $V_C$.

**SOLUTION:** Let all sources be zero. The outcome is then represented by figure E2.3-1(b) for which $V_S$ becomes a short-circuit and $I_S$ becomes an open circuit.

The topology of figure 2.3-1(b) can also be mentally reoriented to the form shown by figure 2.3-1(c). This reorganization is not essential and mostly just for conceptual convenience. For reference it might be noted each of the resistances are between the same nodes as they were in figure 2.3-1(b).
The last figure lets us ply our skills at assessment of a resistance network by inspection, for which we should take note that

\[
\frac{R_1}{R_2} = \frac{2.0}{0.5} = 0.4 \text{k}\Omega
\]

\[
R_2 + 0.4 \text{k}\Omega = 1.0 + 0.4 = 1.4 \text{k}\Omega
\]

\[
\frac{R_4}{1.4 \text{k}\Omega} = \frac{1.0}{1.4} = 0.58 \text{k}\Omega \text{ (approximately)} \quad \text{or} \quad R_{th} = 0.58 \text{k}\Omega
\]

The rest of the story is that either \( I_n \) or \( V_{th} \) must be identified. Since Example 2.3-1 is the same as Example 2.2-1 then \( V_{out} = V_C = V_{th} \) courtesy of nodal analysis.

(for which) \( V_{th} = V_C = 4.5 \text{V} \) i.e. \( V_{th} = 4.5 \text{V} \)

Since the Thevenin equivalent form is equivalent to a non-ideal source, then with load \( R_L \) it will form a voltage divider with voltage across the load of

\[
V_L = \frac{R_L}{R_{th} + R_L} \times V_{th} = \frac{R_L}{R_{out} + R_L} \times V_{th} \quad (2.3-2)
\]

Equation (2.3-2) also acknowledges that \( R_{th} \) is another name for output resistance \( R_{out} \).

If an electrical source is applied to a resistance \( R_L \), a flow of energy results and heats up the load, sometimes to incandescence. Electrical energy is of the form of charge stored under voltage, i.e.

\[
\text{w} = \text{Q} \times \text{V} \quad (2.3-3)
\]

where \( w \) = energy (work energy equivalent) and \( Q \) = quantity of charge (\( w \) and \( Q \) are the conventional symbols) and \( V \) is the voltage relative to the GND reference.
For the flow of charge at potential $V$, the power = rate of energy transferred is

$$P = \frac{dw}{dt} = V \times \frac{dQ}{dt} = V \times I$$  \hspace{1cm} (2.3-4)$$

A less likely option is one in which charge does not flow but is raised or lowered to a different potential. But in circuits for which there is current-flow, equation (2.3-4) prevails and is an axiom of circuits.

In the case of in which energy is dissipated in a resistance, Ohm’s law states that current is proportional to voltage and therefore the power dissipation is then

$$P = V \times I = V \times \frac{V}{R} = \frac{V^2}{R}$$  \hspace{1cm} (2.3-5a)

or (alternatively)  \hspace{1cm} $$P = V \times I = IR \times I = I^2R$$  \hspace{1cm} (2.3-5b)

Energy dissipated by a resistance results in heat. One of the earliest applications of electrical power was to heat a (vacuum-shielded) filament to incandescence. Consequently, electric power found immediate utility as a smoke-free form of illumination, thereby economizing on a lot of fossilized hydrocarbons and also considerably reducing the risk of residential fires.

**EXAMPLE 2.3-2:**  (a) Determine the Thevenin equivalent voltage and resistance $R_{th}$ for the circuit shown.

(b) Determine the voltage $V_L$ if the load resistance is

(1) $R_L = 6.0k\Omega$

(2) $R_L = 1.0k\Omega$

(c) Determine the power dissipated in each of the load resistances of part (b)

**SOLUTION:**  (a) With the load omitted (i.e. no load) this circuit is a simple voltage divider and may be resolved by inspection. In which case $V_{out} = V_{th} = 5.0V$.

And with the source $V_{S1} = 0$ the upper rail is shorted to GND and  \hspace{1cm} $R_{th} = 12k\parallel 6k = 4k\Omega$. (by inspection)

(b) (1) For $R_L = 6.0k$  \hspace{1cm} $V_L = \frac{6}{4+6} \times 5.0 = 3.0V$

And for (2) $R_L = 1.0k$  \hspace{1cm} $V_L = \frac{1}{4+1} \times 5.0 = 1.0V$
(c) The power $P_L$ that is dissipated in $R_L$ for each case will then be

1. $R_L = 6.0k : \quad P_L = \frac{V^2}{R_L} = \frac{3.0^2}{6k} = 1.5mW$

2. $R_L = 1.0k : \quad P_L = \frac{1.0^2}{1k} = 1.0mW$

Example 2.3-2 might raise the question: For what resistance $R_L$ is the power transfer to the load = maximum?

If we undertake a little fun algebra then

$$P_L = \frac{V^2}{R_L} = \left(\frac{R_L}{R_{th} + R_L}V_{th}\right)^2 \times \frac{1}{R_L} = \frac{R_LV_{th}^2}{(R_{th} + R_L)^2}$$

which is a maximum when $\frac{\partial P_L}{\partial R_L} = 0$. So after a little fun calculus

$$\frac{\partial P_L}{\partial R_L} = 0 = \frac{(R_{th} + R_L)^2 - 2R_L V_{th}^2}{(R_{th} + R_L)^3} = \frac{R_{th} - R_L}{(R_{th} + R_L)^3} V_{th}^2$$

which shows that the maximum $P_L$ occurs when $R_L = R_{th}$ and will be

$$P_L(\text{max}) = \frac{1}{4} \frac{V_{th}^2}{R_L} = \frac{1}{4} I_L V_{th} \quad \text{at } R_L = R_{th}$$

Equation 2.3-7 is called the **maximum power transfer theorem**.

**EXAMPLE 2.3-3:** (a) What is the maximum power dissipated by the circuit of example 2.3-2?

(b) And compare to pspice

**SOLUTION:** $P_L = \frac{1}{4} \frac{V_{th}^2}{R_L} = \frac{1}{4} \times \frac{5.0^2}{4k} = 1.563mW$

In pspice $P_L$ vs $R_L$ is shown as a plot, with maximum at $P_L = 1.56mW$. 
Maximum efficiency is a collateral issue but is not the same as maximum power transfer. Efficiency is given by

$$\eta = \frac{P_L}{P_S}$$  \hspace{2cm} (2.3-8)

Where $P_S$ is the power developed by the source $= I_L \times V_{source} = I_L \times V_{th}$. So equation (2.3-8) becomes

$$\eta = \frac{I_L \times V_L}{I_L \times V_{th}} = \frac{V_L}{V_{th}} = \frac{R_L}{R_{th} + R_L}$$  \hspace{2cm} (2.3-9)

since the Thevenin (source) resistance $R_{th}$ and the load resistance $R_L$ form a voltage divider. If equation (2.3-9) is rewritten as

$$\eta = \frac{1}{1 + \frac{R_{th}}{R_L}}$$  \hspace{2cm} (2.3-10)

From equation (2.3-10) it should be evident that maximum efficiency (100%) occurs when either $R_L = \infty$ or when $R_{th} = 0$.

For the case of maximum power transfer (for which $R_L = R_{th}$) the efficiency $\eta = 50\%$.  

---

**Figure E2.3-3(a)** $P_L$ vs $R_L$ with answers to exercise 2.3-2 marked by cursors.

**Figure E2.3-3(b)** Same as (a) but with decade resistance scale and peak marked by cursor.
2.4 SOURCES and SUPERPOSITION

Courtesy of the network laws series paths relate to a sum of voltages. Parallel paths relate to a sum of currents. This concept extends to sources. Voltage sources in series add. Current sources in parallel add.

On the other hand, voltage sources may not be deployed in parallel and current sources may not be deployed in series. If done so it creates a contention. Circuit simulation software will reject circuit topologies that have these faults and make snide error messages about the intelligence of the perpetrator.

But by Thevenin’s theorem and Norton’s theorem the outcome of any single source within the circuit will result in a Thevenin equivalent $V_{th}$ or an equivalent Norton $I_{n}$. And if there is more than one source then their individual contributions will add, i.e.

$$V_{th} = V_{th1} + V_{th2}$$  \hspace{1cm} (2.4-1a)

or $$I_{n} = I_{n1} + I_{n2}$$  \hspace{1cm} (2.4-1b)

This is called the **principle of superposition**. Superposition is a property of linear systems. And it also serves as a simplification technique for circuit topologies with more than one embedded source or I/O networks with more than one input.

Consider example E2.3-1 (redeployed as Example E2.4-1.)

**EXAMPLE 2.4-1:** Determine the Thevenin equivalents $R_{th}$ and $V_{th}$ for the circuit of Example 2.2-1 if the output is at $V_C$.

**SOLUTION:** Let all sources be zero. The outcome is then the same as example 2.3-1 for which $V_S$ becomes a short circuit and $I_S$ becomes an open circuit. Then by inspection

$$R_{th} = 1.4k||1.0k = 0.58 \, k\Omega$$

**Figure E2.4-1(a) Example network**

(1) Let $V_S = 0$ and $I_S \neq 0$. The network will then collapse to that of figure E2.4-1(b)

The resistance inside the dashed line box is the same as $R_{th}$, which means that figure E2.4-1(b) simplifies to a Norton equivalent. Then the Thevenin voltage for figure E2.4-1(b) will be

**Figure E2.4-1(b) Example network collapsed by $V_S = 0$.**
\[ V_{th1} = I_S \times R_n = 2mA \times 0.58k = 1.167V \]

(2) Let \( I_S = 0 \) and \( V_S \neq 0 \). Then the network will collapse to the form shown by figure E2.4-1(c).

The resistance inside the dashed line box is

\[ = 0.5k + 2k||2k = 1.5k \Omega \]

And therefore \( V_a = \frac{0.5k}{1.5k} \times 5.0 = \frac{1}{3} \times 5.0 \)

And so \( V_{th2} = V_a + \frac{1}{2} \times (5.0 - V_a) = \frac{2}{3} \times 5.0 = 3.333 \text{ V} \)

**Figure E2.4-1(b)** Example network collapsed by \( I_S = 0 \).

And then \( V_{th} = V_{th1} + V_{th2} = 1.167 + 3.333 = 4.5 \text{ V} \)

= same as that determined by nodal analysis via Example 2.2-1.

Other techniques associated with network simplification are source equivalence and source absorption using the Thevenin-Norton equivalence given by figure 2.3-3.

Consider the following example

**EXAMPLE 2.4-2**: Find:

(a) the Thevenin equivalent for the circuit shown using the source transformation and absorption technique

and (b) determine the maximum power transfer possible for this circuit.

**Figure E2.4-2(a)** Example multi-source circuit
**SOLUTION:** (part (a) is represented by Figure E2.4-2(b))

(1) The source to the left can be converted to Norton form with $I_{n1} = \frac{20}{4k} = 5.0\,mA$ (= transformation)
(2) The two current sources are in parallel and add to give $I_{n2} = I_{n1} + (-2\,mA) = 3.0\,mA$ (= absorption)
(3) The short-circuit current at the output $I_n = \frac{1/8}{1/8 + 1/4} \times 3.0\,mA = 1.0\,mA$
(4) The Norton-Thevenin conversion gives $V_{th} = 1.0\,mA \times 3k = 3.0\,V$

And the $R_{th} = 4k || (8k + 4k) = 3.0\,k\Omega$ for all sources = 0.

(b) The maximum power to $R_L$ is when $R_L = 3.0k\Omega$ and is $P_L = 0.25 \times (1.0\,mA \times 3.0\,V) = 0.75\,mW$

As a snake check this example can also be done by superposition (Example 2.4-3).

**EXAMPLE 2.4-3:** Find the Thevenin equivalent for the circuit shown using superposition.

**Figure E2.4-3(a)** Example circuit
SOLUTION:

Current source = 0, equivalent to open circuit.

\[ V_{th1} = \frac{4k}{12k + 4k} \times 20 = 5.0\text{V} \]

Voltage source = 0, equivalent to short circuit.
Current through 4k resistance at output under no load at output

\[ I_2 = \frac{1/12}{1/4 + 1/12} \times -2mA = -0.5mA \]
\[ V_{th2} = -0.5mA \times 4k = -2\text{V} \]

So \[ V_{th} = V_{th1} + V_{th2} = 5.0 + -2.0 = 3.0\text{V} \]
And for all sources = 0. \[ R_{th} = 4k||(8k + 4k) = 3.0\Omega \]

The reality of having at least two methods to achieve the same result is always a benefit. It gives a snake check. If different results occur then both (or all) assessments should be revisited.

The two examples also show the two instances in which the current source may be parsed. For example 2.4-2, the Norton equivalent analysis is accomplished with the output shorted (as is required for Norton analysis). But for example 2.4-3, the contribution of the current source was assessed with the output open consistent with the Thevenin equivalent analysis that \( V_{th} \) is the open-circuit output voltage.

2.5 TWO-PORT NETWORKS AND DEPENDENT SOURCES

The Thevenin and Norton theorems are oriented toward a ‘black-box’ equivalent circuit. These theorems focus on the output as a source equivalent, either of the form of its open-circuit voltage (= \( V_{th} \)) or its short-circuit current (= \( I_n \)). The source equivalents are otherwise limited by resistance \( R_{th} = R_n \) and obedient to the relationship \( R_{th} = V_{th} / I_n \).

However, the more general form of a ‘black-box’ equivalent is one in which the box has both an input port and an output port, i.e. a two-port network form. Inputs are usually of the form of signals that may be (1) from a sensor or (2) from a previous ‘black-box’ stage.

If the black box has more than two inputs or more than two outputs it can be constructed from individual two-port networks in parallel, as indicated by figure 2.5-1.
The transfer relationship between input and output indicates the need to identify a transfer component, a.k.a dependent source. A dependent source is like a Thevenin/Norton $V_{th}$ or $I_n$ source except that it is controlled from elsewhere in the circuit and is zero if the electrical measure at the controlling site is zero. The control site is like an input port, and probably is. Dependent sources therefore are defined as two-port type components and fall into the category of one of four types, as represented by figure 2.5-2.

Figure 2.5-2. Dependent sources

Where:
- VCT = voltage-to-current transducer
- VVT = voltage-to-voltage transducer
- CCT = current-to-current transducer
- CVT = current-to-voltage transducer

Figure 2.5-2 represents ideal transfer components with output properties that are not unlike the independent sources referenced so far. But if they are framed in terms of input and output ports they are expected to be consistent with the Thevenin and Norton theorems. The output port assume a Thevenin/Norton source designated either as $v_{out}$ or as $i_{out}$ with output resistance $R_{out} = R_{th} = R_n$. And as defined by the theorems the output resistance is defined under the criterion that that all sources = 0 to include the input.
It is also not unreasonable to assume that the two-port I/O network is unidirectional, or nearly so, in which case the input port will have no reflexive source component hiding within and its only feature will be input resistance $R_{in}$. The transfer characteristics of the two-port I/O forms are shown by figure 2.5-3 and reflect the context of an $R_{in}$ and an $R_{out}$.

It is also not uncommon for the generic types of two-port networks to have a common ground for both input and output.

**Figure 2.5-3.** Generic two-port network forms

Figures 2.5-2 and 2.5-3 and the text description also emphasizes that the two-port form is oriented more toward signals (represented by lower case) rather than level values (as represented by upper case). In this respect the two-port network is a signal transfer element.

The essential two port network characteristics are the port resistances $R_{in}$, and $R_{out}$ and a (signal) transfer function. The most common transfer function is $v_{out}/v_{in}$ in which case the two-port network may be designated as a voltage amplifier (regardless of whether it amplifiers or not). The next most common transfer function is $i_{out}/i_{in}$, i.e. current amplifier. All transfer function types are related to one another through input and output resistances $R_{in}$ and $R_{out}$.

For example the current transfer function and the voltage transfer function are related by

$$\frac{i_{out}}{i_{in}} = \frac{v_{out}}{v_{in}} R_{out} = \frac{R_{in}}{R_{out}} \times \frac{v_{out}}{v_{in}}$$

(2.5-1)

The four types of dependent sources given by figure 2.5-2 also reflect the four different types of transfer functions even though the internal transducer may not be the same type as its two-port outcome.

Input resistance and output resistance are not alike, however. They only look like it. They will both form voltage dividers with the external resistances. And they will both serve to translate one type source to another type source. But input resistance $R_{in}$ is a load resistance whereas output resistance is a source resistance.

$R_{out}$ fulfills the role that it does since it is defined in terms of open circuit voltage $v_{out}$ and short-circuit current $i_{out}$, respectively, as represented by equation (2.5-2).
\[ R_{\text{out}} = \frac{v_{\text{OC}}}{i_{\text{SC}}} = \frac{v(R_L = \infty)}{i(R_L = 0)} \]  

Equation (2.5-2) is nothing other than a repeat of the Thevenin/Norton theorems with an emphasis on the character of \( R_{\text{out}} \).

Load, source, and I/O (input and output) resistance will each form voltage dividers with their source/load associates. By way of example, when a load \( R_L \) is connected to the output port, then \( R_{\text{out}} \) and \( R_L \) form a voltage divider which has (signal) transfer ratio

\[ \frac{v_L}{v_{\text{out}}} = \frac{R_L}{R_{\text{out}} + R_L} \]  

The role of the I/O resistances and signal transfer ratios are of considerable significance in the transfer relationship of power from input to load as represented by figure 2.5-4 and equation (2.5-4)

**Figure 2.5-4.** Power transfer from source to load via two-port interface

The power transfer ratio is

\[ \frac{P_L}{P_{\text{in}}} = \frac{v_L \times i_L}{v_{\text{in}} \times i_{\text{in}}} = \frac{v_L}{v_{\text{in}}} \times \frac{i_L}{i_{\text{in}}} = \frac{v_L}{v_{\text{in}}} \times \frac{v_L/R_L}{v_{\text{in}}/R_{\text{in}}} \]

\[ = \left( \frac{v_L}{v_{\text{in}}} \right)^2 \frac{R_{\text{in}}}{R_L} \]  

(2.5-4)

where \[ \frac{v_L}{v_{\text{in}}} = \frac{R_L}{R_{\text{out}} + R_L} \times \frac{v_O}{v_{\text{in}}} \]
**EXAMPLE 2.5-1**

An echolocation sensor is characterized by signal voltage $v_S = 10\text{mV}$ or short-circuit current $i_{SS} = 0.05 \mu\text{A}$. If connected to an amplifier stage with input resistance $R_{in} = 50k\Omega$, output resistance $R_{out} = 2.5k\Omega$, and open-circuit signal gain $A_V = 25\text{V/V}$, and drives a load of resistance $R_L = 10k\Omega$ determine

(a) transfer ratio $v_L/v_S$
(b) signal voltage $v_L$ at the output and
(c) power gain $p_L/p_{in}$.

**SOLUTION:**

Source resistance of the echolocation sensor is

$$R_s = \frac{v_S}{i_{SS}} = \frac{10\text{mV}}{0.05 \mu\text{A}} = 200k\Omega$$

Then

$$\frac{v_{in}}{v_S} = \frac{R_{in}}{R_s + R_{in}} = \frac{50}{200 + 50} = 0.2\text{V/V}$$

(for which $v_{in} = 0.2 \times 10.0 = 2.0\text{mV}$)

Using signal ratios

$$\frac{v_{L}}{v_{in}} = \frac{v_{in}}{v_{o}} \times \frac{v_{L}}{v_{o}} = \frac{v_{in}}{v_{o}} \times \frac{R_L}{R_{out} + R_L} = 25 \times \frac{10}{2.5 + 10} = 20 \text{V/V}$$

Then (a) $v_L/v_S = (0.2 \text{ V/V}) \times (20 \text{ V/V}) = 4.0 \text{ V/V}$

And (b) $v_L = (20\text{V/V}) \times 2.0\text{mV} = 40\text{mV}$ (also $v_L = 10 \times 4.0 = 40\text{mV}$)

Therefore (c) the power gain is

$$\frac{p_L}{p_{in}} = \left(\frac{v_L}{v_{in}}\right)^2 \frac{R_{in}}{R_L} = (20)^2 \times \frac{50}{2.5} = 8000\text{W/W}$$

Notice that the two-port network also serves as a means to match compatible resistances. Had the 2-port network been omitted and the signal $v_S$ attenuated by the voltage divider made by $R_s$ and $R_L$ then

$$v_{L2} = \frac{10}{200 + 10} \times 10\text{mV} \approx 0.05\text{mV}$$

with insertion gain

$$\frac{v_{L1}}{v_{L2}} = \frac{40\text{mV}}{0.05\text{mV}} = 800 \text{V/V}$$

The two-port network emphasizes the relationships of transfer ratios and the fact that the network may have capability to add or lose power as the signal is transferred across the network. Sometimes it is many orders of magnitude, as represented by example 2.5-1. And that suggests that the signal gain or loss
should also be identified in order-of-magnitude measure. For electrical circuits and the history associated with applications thereto this measure is in terms of a unit called the dB (decibel).

dB measure is identified first and foremost in terms of the impact on the application, which is invariably the (energy-effect) relationship of power. So one order-of-magnitude is 10 dB, two orders-of-magnitude is 20 dB, three orders of magnitude is 30 dB, etc. So order-of-magnitude measure in dB for a two-port network is

\[
\text{(dB measure)} = 10 \log \left( \frac{p_{\text{out}}}{p_{\text{in}}} \right)
\]

(2.5-5)

So for Example 2.5-1 the power gain would be

\[
\text{(db measure)} = 10 \log (8000) = \text{39 dB}
\]

Since factors of two are after important we often single them out in dB measure, i.e.

\[
10 \log (2) = 3 \text{dB}
\]

(2.5-6)

To add to the context of dB measure, take note that the power ratio has a quadratic relationship with the amplitude ratio as represented by equation (2.5-4). So a factor-of-10 increase in the amplitude ratio corresponds to a factor increase in the power ratio of 100, or 20 dB.

So dB measure of amplitude ratios then has an effect of

\[
\text{(db measure)} = 20 \log \left( \frac{v_{\text{out}}}{v_{\text{in}}} \right)
\]

(2.5-7)

Often the amplitude ratios are identified on an equal footing as the power ratio factors, and so equation (2.5-7) may prevail. And if so then

\[
3 \text{dB (for amplitude)} = 20 \log \sqrt{2}
\]

(2.5-8)

Amplitude factors of \(\sqrt{2}\) are denoted as a 3 dB reference level.
PORTFOLIO and SUMMARY

\[ I = GV \quad \text{Ohm's law} \]
\[ V = IR \]
\[ G = \sigma \times \frac{A}{L} \]
\[ R = \rho \times \frac{L}{A} \]

\[ \frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \]
\[ R_{eq} = R_1 + R_2 + R_3 \]

Voltage divider:
\[ V_B = \frac{R_2}{R_1 + R_2} \times V_A \]

R-2R ladder

\[ \sum I_K = 0 \]
\[ \begin{bmatrix} G_{I1} & \cdots & G_{IN} \\ \vdots & \ddots & \vdots \\ G_{I1} & \cdots & G_{IN} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_N \end{bmatrix} = \begin{bmatrix} I_{S1} \\ \vdots \\ I_{SN} \end{bmatrix} \]

Nodal analysis

\[ \sum V_K = 0 \]
\[ \begin{bmatrix} R_{I1} & \cdots & R_{IN} \\ \vdots & \ddots & \vdots \\ R_{I1} & \cdots & R_{IN} \end{bmatrix} \begin{bmatrix} I_1 \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} V_{S1} \\ \vdots \\ V_{SN} \end{bmatrix} \]

Loop (mesh) analysis

Sources:
Voltage source \( R_{out} = 0 \)
Current source \( R_{out} = \infty \)
Power dissipated in a resistance

\[ P = IV \]
\[ = \frac{V^2}{R} \]
\[ = I^2 R \]

Thevenin and Norton theorems:

\[ I_n = \frac{V_{th}}{R_{th}} \quad V_{th} = I_n R_n \quad R_n = R_{th} \]

Maximum power transfer:

\[ P_L = \frac{1}{4} \frac{V_{th}^2}{R_L} \]
\[ = \frac{1}{4} I_n V_{th} \]

at \( R_L = R_{th} \)

Maximum efficiency for \( R_{th} \ll R_L \)

Figure A-1.1 pspice rendition, maximum power transfer

Superposition (Thevenin/Norton outputs):

\[ V_{th} = V_{th1} + V_{th2} \]
\[ I_n = I_{n1} + I_{n2} \]

Dependent sources options

Two-port transfer circuits

\[ R_{in} = \frac{v_{in}}{i_{in}} \]
\[ R_{out} = \frac{v_{out}}{i_{out}} \]
\[ R_L = \frac{v_L}{i_L} \]
\[ v_L = \frac{R_L}{R_{out} + R_L} v_{out} \]
\[ i_L = \frac{R_L}{R_{out} + R_L} i_{out} \]
\[ v_L = \frac{R_L}{R_{out} + R_L} v_{in} \]
\[ i_L = \frac{R_L}{R_{out} + R_L} i_{in} \]
\[ p_L = v_L \times i_L = \frac{v_L}{v_{in}} \times i_L \]
\[ p_L = \frac{v_L}{v_{in}} \times i_L \]
\[ p_L = \left( \frac{v_L}{v_{in}} \right) R_{in} \]

dB measure:

\[ (\text{dB measure}) = 10 \log \left( \frac{p_{out}}{p_{in}} \right) \]
\[ = 20 \log \left( \frac{v_{out}}{v_{in}} \right) \]

3dB (for amplitude) = 20 log \( \sqrt{2} \) corresponding to 3dB (for power) = 10 log (2)