CHAPTER 9. DIODES and DIODE CIRCUITS

9.1 INTRODUCTION TO SEMICONDUCTOR ELECTRONICS

The earliest form of non-linear electronics was not based on semiconductor electronics but on devices in which the flow of electrons was contained within a vacuum envelope, or tube. Vacuum tubes were intricate and interesting, but were bulky, hard to make, and easily broken. And their cathode filaments had a limited lifetime. If we should wish to work in outer space where a vacuum is readily available they might make a resurgence. But here on the earth, with its oxygen-nitrogen atmosphere and the discovery that most electronics could be accomplished using semiconductors, vacuum tubes became an obsolescent artifact in the history of electronics.

Semiconductors are interesting and unique in that they may be alloyed to provide an excess of charge carrier densities according to 'doping' levels of alloyed impurities. Furthermore the impurity alloying can be patterned using masks, particularly when the impurities can be injected and laid down by means of ion guns and molecular beams and other such weaponry. In addition to these aspects, impurity alloying invites the context of two types of charge-carriers, (1) electrons and (2) holes (what??). Excess electron densities afforded by 'donor' impurities speak for themselves. The nomenclature that we identify as 'holes' is peculiar to the fact that we are using a solid-state lattice as a medium which will accommodate the absence of an electron at the atomic sites defining the lattice. The absence of an electron represents a positive charge site that may be traded around with much of the same mobility as that of a conduction electron except with an electronic charge measure of $+q$ instead of a $-q$ measure.

The secret, of course, is that semiconductors are a material that is neither metal nor insulator. They are characterized by a band-gap between (1) the valence energies that bind the crystal together and (2) the higher energies in which electrons are not bound but are (reasonably) free to roam throughout the material. The physics is entertaining, as most physics usually is. The band-gap context is shown by figure 9.1-1. If the band-gap is overly large (e.g. $E_G > 5$ ev) the material is then an insulator.

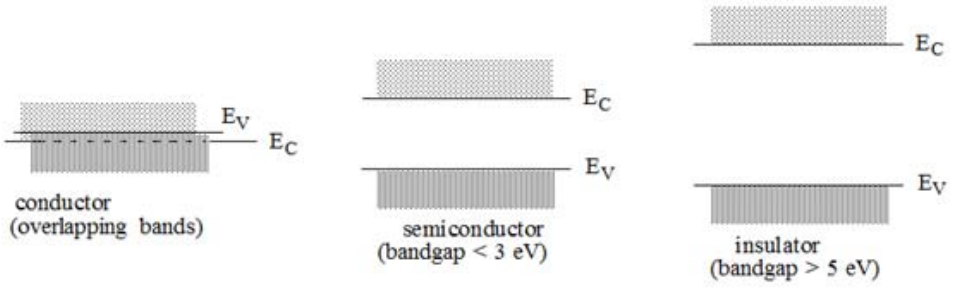
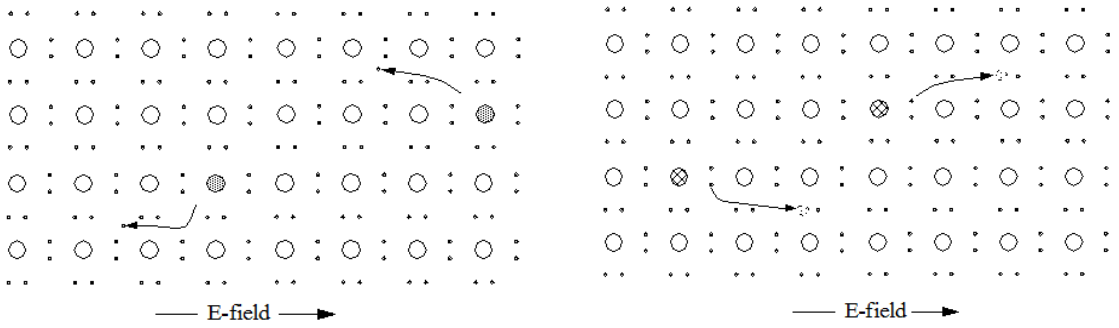


Figure 9.1-1. Band-gap context of semiconductors.

Notice that the higher-energy band is labeled as the 'conduction' band with lower band edge E_C, since electrons at these energies are not strongly bound and can therefore be pushed around by the slightest of E-fields, much like the electrons within a metal. The context is even more emphatic when viewed as a lattice, such as that of Silicon, which is tetravalent, and therefore is bound (covalently) to four nearest neighbors as shown by figure 9.1-2.



(a) Donor impurities under E-field (movement of loose electrons)

(b) Acceptor impurities under E-field (movement of loose holes)

Figure 9.1-2. The Si lattice in 2-dimensions, showing covalent (shared) electrons between atomic lattice nodes. (Actually the lattice is more like that of figure 9.1-4 (a) for which four nearest neighbors are at tetrahedral vertices.)

The two-dimensional representation is most informative since we can look upon the semiconductor in terms of the effect of appropriate impurities. For example, as shown by the figure, if a phosphorus (pentavalent) impurity is introduced into the lattice, its extra valence electron becomes a step-child. It is therefore prone to depart and wander around the neighborhood. On the other hand if a boron (trivalent) impurity is introduced within the lattice it leaves a 'hole' (hence the name). And the hole will skip from one site to the next as neighboring covalent electrons fall into it and leave an absence (hole) at their former home site. Once again the physics is fun, particularly when the lattice structure is introduced, for which the simple band-gap context takes on a periodic geometric context.

But the context is still relatively simple. A hole is very much like the little bubblets that you will see when you drop by your local tavern for a tall cold ginger ale. Notice that bubblets fall upward, whereas pellets fall downward. In the context of semiconductors the gravitational field would be replaced by an electric field for which 'holes' are equivalent to bubblets and the electrons are equivalent to pellets.

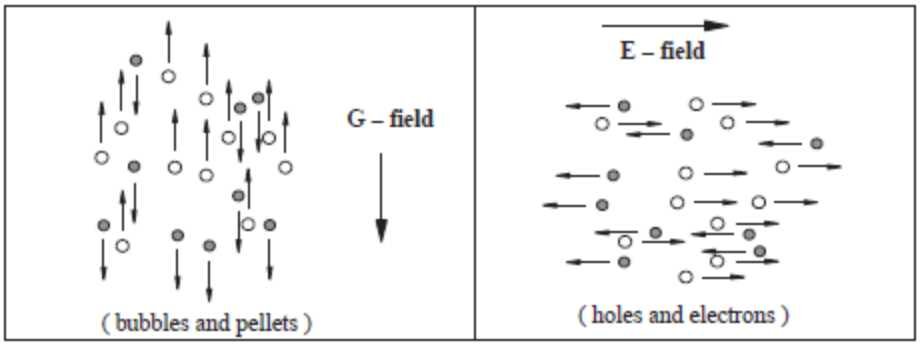


Figure 9.1-3. Holes and electrons analogy to bubblets and pellets.

So semiconductors are an awesome material. Unlike anything else they have two types of charge carriers (electrons and holes). They also have interesting crystalline structures, as represented by figure 9.1-4.

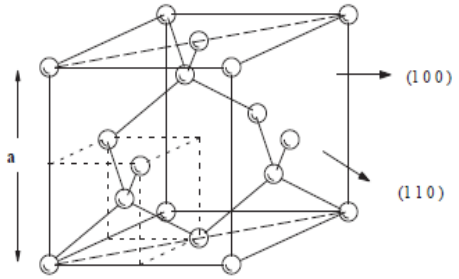


Figure 9.1-4(a) . The Silicon lattice (diamond lattice unit cell). The sub-cell (dashed) is tetrahedral.

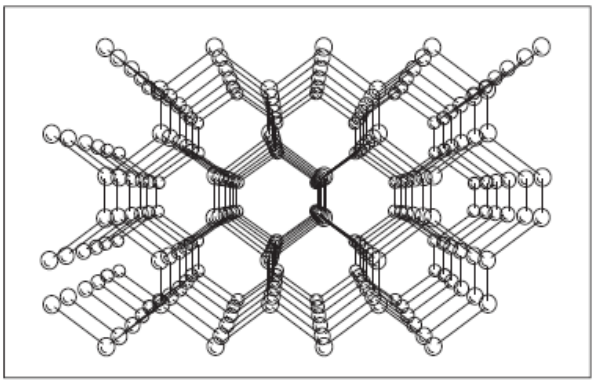


Figure 9.1-4(b). The array of tetrahedrons along the (110) direction of the crystal.

Figure 9.1-4(b) shows the silicon lattice looking from the (110) direction and shows that ballistic channels exist in this direction. When an integrated circuit is formed, the transistor devices are oriented so that the electron (or hole) flow falls along the (110) direction. And even though the intent at this point is to examine semiconductors as a solid-state material, the eventual calling will be to think about circuits that are formed by patterning the semiconductor material and interconnect layers as an integrated circuit.

It is appropriate that the nomenclature reflect the types of charge carriers that are induced by the impurity alloying. And so those materials that have impurity doping which contributes electrons (also called donor impurities) are identified as 'n-type' (i.e. suffused with negative charge carriers). Those materials which accept electrons (and leave holes) (and are also called acceptor impurities) are identified as 'p-type' (i.e. suffused with positive charge carriers).

And thus we can pattern the semiconductors in terms of their electrical properties as reflected by the type of charge carriers. It only takes a minute level of impurities (usually on the order of $1{:}10^6$) to define the character of the semiconductor. Almost everything associated with semiconductor electronics is identified in terms of the incidence and presence of *pn* junctions.

9.2 *PN* JUNCTIONS

The metallurgical context of the *pn* junction is straightforward, although there are all kinds of *pn* junctions. Semiconductor junctions have variations according to impurity profiles, geometrical options, types of impurities and type of semiconductor. There are probably as many different types of *pn* junctions as there are different taxonomies of insects. There are even types of junction that aren't *pn* junctions but have a lot of the properties thereto. But no matter how clever the construct may be, the simplest *pn* junction is good with the physics. The nominal manufacturing context is shown by figure 9.2-1. The rest of the story is shown by figure 9.2-2, which is a slice across figure 9.2-1. The electrical properties (characteristics) are the primary subject of interest to the electrical engineer.

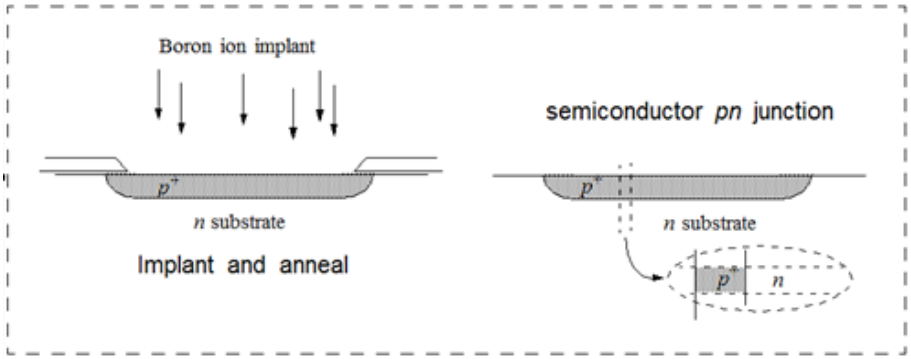


Figure 9.2-1. Ion implantation process for *pn* junction

Notice that figure 9.2-1 also introduces the concept of counter-doping, in which case it is the excess of impurities that define the type of semiconductor. With counter-doping the lower density impurities sites are filled by the opposite type carrier and no longer contribute to the conduction. So the type (*n* or *p*) is an indication of the majority carriers.

In the vicinity of the junction thermal diffusion will cause electrons to migrate across the boundary from the n-side into hole territory. In doing so the migration leaves behind a layer of uncovered donor sites which become an ionized layer of (+) charges. On the p-side the immigrant electrons fill acceptor sites to the layer depth on the order of microns, creating an ionized layer of the (-) type charge. Consequently the two uncovered layers in the vicinity of the junction boundary induce a formidable built-in electric

field that blocks any further migration of charge across the junction boundary. The built-in field context is a signature of the junction and is represented by figure 9.2-2.

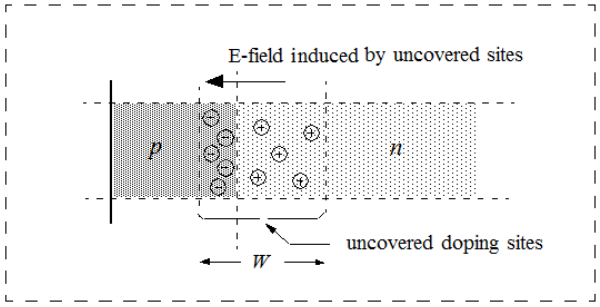


Figure 9.2-2. Uncovered impurity sites in the vicinity of the *pn* junction boundary

This behavior reveals another context of semiconductors, namely that they accommodate the presence of an electric field, much like an insulator. In the vicinity of a *pn* junction the thermal statistics induces an E-field strong enough to crackle were it outside the material. And yet the semiconductor material away from the junction contains sufficient mobile charge carrier densities for good conduction.

Since the two opposite polarity uncovered layers (also designated as the space-charge layer) thickness is on the order of microns the junction E-field is huge. Consider the following example:

EXAMPLE 9.2-1: An abrupt junction has a density of (acceptor)(*p*-type) impurities of $N_A = 10^{16}$ #/cm^3 and a density of (donor)(= *n*-type) impurities of $N_D = 10^{15}$ #/cm^3. (This is called a one-sided junction and is reflected by the illustration). The field develops a voltage difference due to the band-gap of $\phi_B = 0.8$V which uncovers the doping sites to a layer thickness of 0.18μm on the *p*-side and 1.8μm on the *n*-side. (Notice that this gives charge equilibrium). What is the magnitude of the electric field in V/cm?

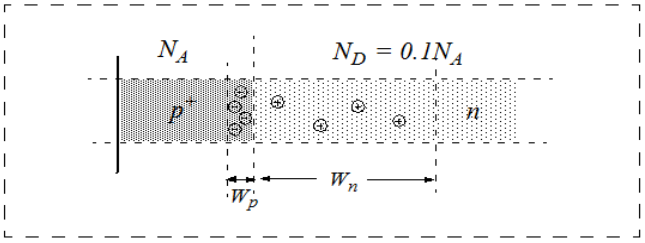


Figure E9.2-1: Example slice across an abrupt (idealized) *pn* junction. Note that charge equilibrium requires that the more lightly-doped uncovered charge layer be much thicker than that for the more heavily doped side. The donor impurities have density $N_D = 0.1 \times N_A$ and so $W_n = 10 \times W_p$.

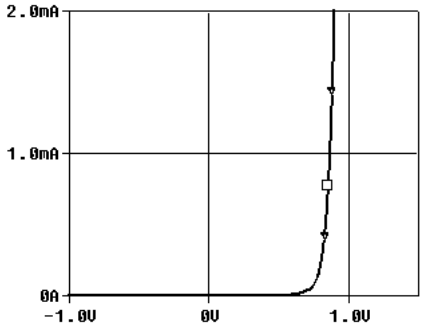
SOLUTION: The average separation of charge = $0.5 \times (W_p + W_n) = 0.5 \times (0.18 + 1.8)\mu m = 1.0\mu m$.

The E-field is then = (0.8V/1.0μm) = 0.8 V/μm = 0.8×10^4 V/cm. = **8.0 kV/cm**

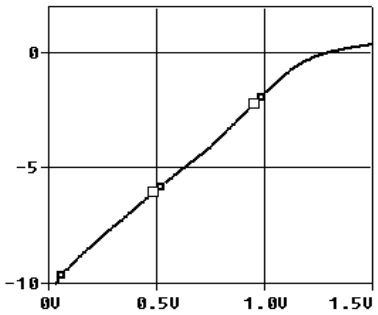
Example E9.2-1 points out that the intrinsic electric field due to the uncovered charge sites in the vicinity of the metallurgical junction is anything but small. This large E-field then serves to block any further migration (= diffusion) of charge across the junction boundary.

However if we should lower the electric field by means of a forward voltage bias $(V_p - V_n) > 0$ the thermal diffusion pressures will cause charge carriers to flood across the junction. Diffusion is a thermal process defined by thermal statistics. The thermal flood has an exponential behavior relative to the quantized thermal energy kT and therefore the charge carrier flow will also be exponential relative to kT/q, as indicated by figure 9.2-2 and by equation (9.2-1).

If $V_{pn} < 0$ (which we also call reverse-bias) the E-field barrier becomes larger and continues to block the diffusion of charge carriers across the junction boundary.



(a) I (V) on linear scale.



(b) I (V > 0) on logarithmic scale.

Figure 9.2-2. I vs V characteristics of the *pn* junction (= pspice rendition of the 1n914 general-purpose high-speed switching diode).

Figure 9.2-2(b) shows that the slope is approximately linear on the logarithmic scale, which is consistent with the exponential behavior of charge carriers flooding across the forward-biased junction.

The basic mathematical form of this response is given by the ideal diode equation

$$I \cong I_S\left(e^{V/nV_T} - 1\right) \qquad (9.2\text{-}1)$$

where V_T is defined as the thermal voltage and I_S is identified as the reverse saturation current. The voltage V is the same as V_{pn}, otherwise called the forward voltage. The thermal voltage relates to the quantized thermal energy kT as

$$V_T = kT/q \qquad (9.2\text{-}2)$$

Where k = Boltzmann constant = 8.62×10^{-5} eV/K and q = magnitude of the electronic charge = 1.602×10^{-19}C = 1.0eV/J. At nominal room temperature 295K the thermal voltage is then

$$V_T \text{ (at } T = 25^{o}\text{C)} = .0254 \text{ V} \qquad \cong .025V \qquad (9.2\text{-}3)$$

The thermal voltage is given an equation number all of its own because the value $\boldsymbol{V_T = .025V}$ is employed for most back-of-the-envelope calculations.

The parameter n is called the emission coefficient and is the principal reason why the ideal diode equation is not linear for the entire region of $I(V > 0)$. In the vicinity of the most likely region of operation $0.7\text{V} < V < 0.9\text{V}$, emission coefficient n approximately = 1. For lower voltages $n = 2$ (approximately). For voltages higher than 1.2V the resistance of the semiconductor material begins to dominate and the $I(V)$ is linear rather than exponential (which shows up as a roll-off on the logarithmic scale). It should be apparent that the circuit simulator is using more comprehensive mathematical models than just equation (9.2-1) to provide the best possible representation of the diode. So the ideal diode equation is only the first-order part of the story.

The electrical behavior of the junction when it is employed as a circuit component suggests the symbol shown by figure 9.2-3(b). It looks like an arrowhead that points in the direction of forward (also called the 'easy') current flow, consistent with figure 9.2-2.

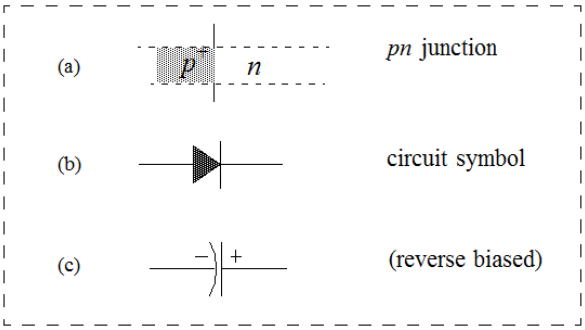


Figure 9.2-3. Physical context and circuit symbol for *pn* junction (diode).

To be fair, minority-carrier current does flow in the reverse-bias direction. It even increases a tad as the reverse bias is increased (as must always be true). It is important to note that reverse-bias current is on the order of $I_S = 10^{-15}\text{A} = 1.0$ fA, depending on the area of the junction. This level of current is less than that for many insulators of like area and tells us that the reverse-biased junction is effectively a very good insulator. For the 1n914 diode $I_S = 16.8 \times 10^{-20}\text{A}$, which is about two orders of magnitude smaller than the conductance of the air in the vicinity of the diode.

The symbolic context also identifies that the junction in reverse-bias is a capacitance, inasmuch as there is a separation of charge and virtually no leakage current. But the junction is also more than a simple plate capacitance because a greater reverse-bias increases the built-in field and uncovers more charge. Hence the layer thicknesses W_n and W_p increase proportionally and therefore the capacitance decreases with the application of more voltage.

Consequently the capacitance of a junction in reverse-bias is voltage dependent. For the (ideal) abrupt junction the behavior is approximately

$$C_J = C_{J0} / \left[1 + V_R / \varphi_J\right]^{MJ} \qquad (9.2\text{-}4)$$

This is a Big deal because a voltage-variable capacitance then will have a time constant that can be controlled electronically and then can readjust circuit tuning by use of feedback.

It should also be noted that once the charge carriers are injected across the junction boundary and flow into the opposite type of semiconductor territory they will recombine with their opposite number at a rate determined by a recombination time constant τ_R. Unfortunately the recombination time constants are usually not as fast as the higher speeds at which we desire to switch the diode on and off, and the lag gives a commutation effect that limits the ON/OFF time response of the device.

9.3 DIODE CONDUCTANCE MODELS FOR CIRCUIT ANALYSIS

The diode is so named because its vacuum tube forebear had two electrodes. The *pn* junction is the two-terminal semiconductor equal and it may exist as either a discrete device or as an included part of another device within a fabricated integrated circuit.

Using Newton-Rhapson iterative techniques, circuit simulation software can accomplish the mathematics of section 9.2 very handily. But the non-linear equations that define the physics are not tractable to the quick analysis necessary for making design decisions. Their use by an engineer is worthwhile only for defining circuit software processes and their use otherwise would be mostly a disciplinary exercise. Less-accurate piece-wise linear models are completely adequate for design assessment of circuits containing diodes and the models of choice are indicated by figures 9.3-1(b) and (c).

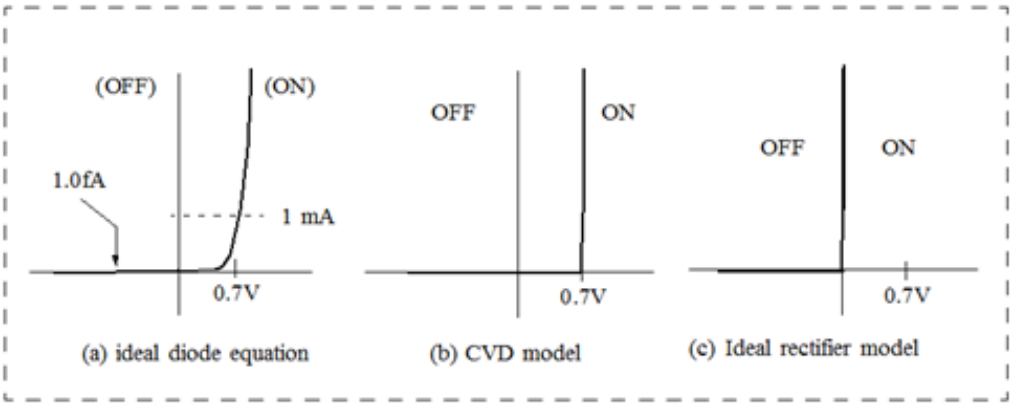


Figure 9.3-1. Circuit analysis conductance models of the diode. (A '1 mA diode' is represented)

The first one (a) is the ideal diode equation and is only shown for the context of 'ON' and 'OFF' conduction modes. The second one (b) assumes that once a threshold level $V = V_\gamma$ is reached, the diode is 'ON', the forward conductance (slope) is infinity, and the forward current can be anything > 0. The last

model (c) is called the 'rectifier' model of the diode and treats it strictly as an ON-OFF device, depending on the polarity. None of these models tell the whole truth, not even the ideal diode equation, but they are good enough for a rough assessment of the circuit. If more accuracy is desired the circuit simulator can be called forth to render its analysis.

And this context is the benchmark of non-linear electronics. The *pn* junction is everywhere and figures into other semiconductor devices of like character and similar non-linearity. As a discrete component and as an embedded component it will adopt the diode symbol of figure 9.2-3(b). And for the sake of the simplest and most direct context its electrical character will employ one of the models of figure 9.3-1, even within the circuit simulator.

For lower voltages, usually less than 10V, the second model in figure 9.3-1 is preferred. It goes by several names, the most common being the 'CVD' (common voltage drop) model, so named because a voltage V_γ will fall across the diode when it is in its forward conducting state. The usually accepted value is $V_\gamma = 0.7\text{V}$ as shown by figure 9.3-1. This is a distinct untruth, since V_γ should depend on the level of current. But for an initial engineering assessment we should accept it without complaint.

Note that the last two models allow us to fall back to an assessment of conductance paths in terms of linear circuit analysis. For the context of currents and voltages the circuit is then resistance/conductance network and the mathematics is simple and direct.

Consider the following example.

EXAMPLE 9.3-1: Diode as a conducting element and the use of the CVD model. Determine electrical facts I_1 and V_1.

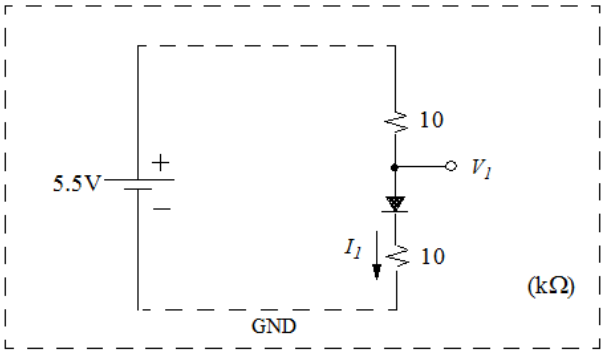


Figure E9.3-1. Diode as a component with a voltage loop.

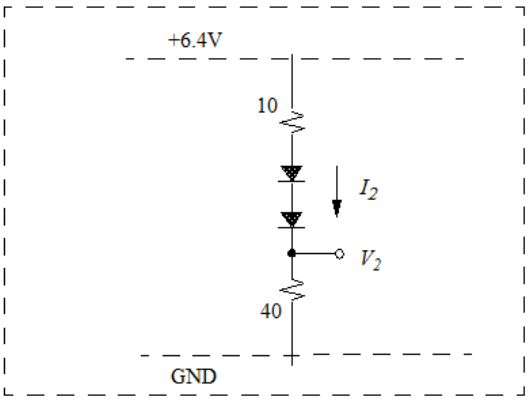
SOLUTION: Using mesh analysis around the loop $I_1 = \dfrac{(5.5-0.7)}{(10+10)} = \underline{\mathbf{0.24\text{mA}}}$

$V_1 = 0+10\times 0.24+0.7 = \underline{\mathbf{3.1\text{V}}}$

Although the example was simple and direct it also suggests that the voltage loop and DC voltage source are an aside to the rest of the circuit and may be treated as ideal batteries with short-circuit current able to forge a wrench or melt down a battleship if so desired.

As a simplification the voltage sources will be replaced voltage supply 'rails', much like we might see if we laid the circuit components down on a printed circuit board or within an integrated circuit. And that brings us to another example, just like that of example 9.3-1, except different.

EXAMPLE 9.3-2: Diodes between voltage rails and analysis by inspection. Find I_2 and V_2.



By inspection

$I_2 = \underline{\mathbf{0.1\,mA}}$

$V_2 = \underline{\mathbf{4.0V}}$

(or otherwise if not, then)

$$I_2 = \frac{(6.4 - 2\times 0.7)}{(10+40)} = 0.1 \text{ mA}$$

$$V_2 = 0 + 10\times 0.24 + 0.7 = 4.0 \text{ V}$$

Figure E9.3-2. Diode string and analysis by inspection

The solution context 'by inspection' should not be unfamiliar and truly is the only practical way to do most aspects of circuit analysis. The CVD and the ideal rectifier model permit us to cut to the chase 'by inspection' and acquire values of the electrical facts without cluttering up the analysis with arithmetic.

But also consider that we are dealing with junction diodes that clearly have two 'states' (ON and OFF). The previous examples made the visual assumption that the diodes were 'ON' and that guided the process. The'OFF' state was not considered. But if you were blind you would have to do so, or identify a bias criterion for the ON/OFF state of the diode component.

The bias assessment is therefore a part of the inspection analysis just as much if not more than the rough mathematical analysis. Consider the following example

EXAMPLE 9.3-3: A diode string between voltage dividers. Find V_1, V_2 and I_D.

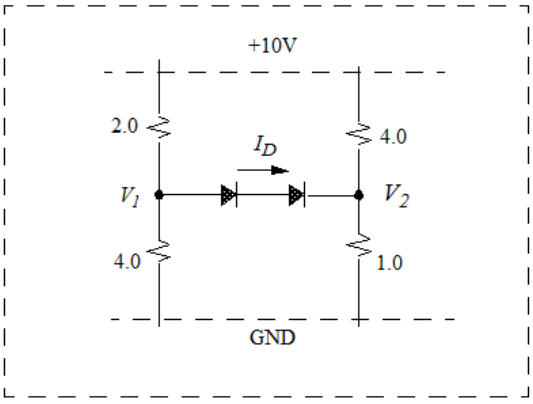


Figure E9.3-3. Diode string and resistance network.

SOLUTION: If you look at the voltage dividers to each side of the diode string it should be evident that V_1 is greater than V_2 *by inspection* since the naked voltage dividers would give $V_1 = 6.67$V and $V_2 = 2.0$V. You do not need the naked values for V_1 and V_2 to affirm that the diode string has no choice but to be conducting. You could even hazard a WAG (wild-eyed guess) as to what voltage values would result since V_1 will be pulled down by the diode current and V_2 will be pulled up. In the analysis of electronic circuits with non-linear elements, even a WAG may be adequate, - even on a quiz, if within 10%.

Turning to mathematics and nodal analysis at V_1 and V_2, respectively, we get

$$\textbf{V1:} \quad V_1(0.5+0.25)-0.5\times10+I_D=0 \qquad \text{and } V_1 = V_2 + 2\times0.7$$

$$\textbf{V2:} \quad V_2(0.25+1.0)-0.25\times10-I_D=0$$

$$\text{----------}$$

$$V_2(0.75+1.25)+1.4\times0.75-(0.5+0.25)\times10=0$$

So that $V_2 = \dfrac{(7.5-1.05)}{2.0}$ = **3.23 V** $V_1 = 3.23 + 1.4$ = **4.62 V**

And from the V_2 node equation: $I_D = V_2(0.25+1.0)-0.25\times10$ = **1.53mA**

The network mathematics invited the use of nodal analysis. Nodal analysis gives node voltages. Circuit simulation software accomplishes its assessment by a modified nodal analysis. But even the circuit simulation software has to make a perceptive preliminary assessment of the node voltages before undertaking its iterative numerical analysis.

Diode characteristics and that of their semiconductor cousins are defined by voltage biases. So options on the voltage states are an essential part of the assessment. The rest of the story is associated with effect of

the resistance paths on the node voltages, and the inspection process give the preliminary assessment and identifies which states are true. Consider the following example

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EXAMPLE 9.3-4: Determine I_{D1}, I_{D2} and V_4.

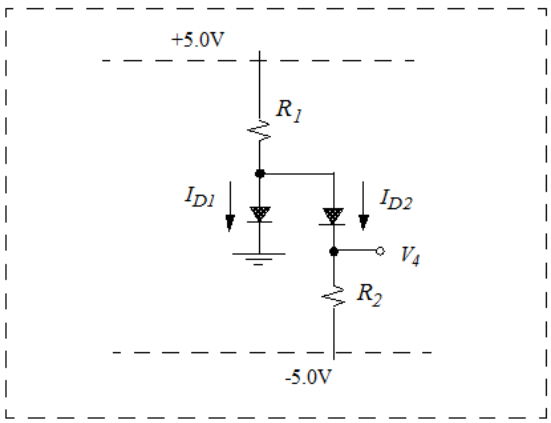


Figure E9.3-4. Two diodes and resistance network.

For: (a) $R_1 = 4.0$, $R_2 = 1.0$ (kΩ)

(b) $R_1 = 1.0$, $R_2 = 4.0$ (kΩ)

SOLUTION: Examine the possibilities. Note that diode D_2 must always be ON since it is oriented correctly for current passing through R_2 and does not care what R_1 and R_2 might be.

(a) For $R_1 = 4.0$ and $R_2 = 1.0$ (kΩ) it appears by inspection that V_4 will be sufficiently negative so that D1 will be OFF. And therefore the current through the string must be

$$I_{D2} = (5 - 0.7 - (-5))/(4.0 + 1.0) \quad = \underline{\textbf{1.86 mA}}$$

Which makes $V_4 = -5 + 1.86 \times 1.0$ = **-3.14 V**

And this makes the voltage *Vx* (penciled in) = -2.44 V

*And this confirms that diode D1 is non-conducting, since it is in reverse bias, just like we presupposed.

So I_{D1} = **0.0mA**

(b) For $R_1 = 1.0$ and $R_2 = 4.0$ (kΩ) it appears by inspection that V_4 will be sufficiently positive so that it is expected that D1 will be ON. And therefore voltage V_4 = **0.0V**,

and the current through R_2 will be $I_2 = I_{D2}$ = **1.25 mA** (by inspection)

and also *Vx* (penciled in) = 0.7V

and therefore the current through R_1 will be $I_{D2} = (5 - 0.7)/1.0$ = 4.3mA

And the current through D1 is 4.3mA – 1.25mA I_{D1} = **3.0mA**

*And this confirms that diode D1 is conducting, (for which. $I_{D1} > 0$) just like we presupposed.

Also note that we can only determine the current through a diode indirectly. So we determine currents through the associated paths and then make use of the law of currents (otherwise known as KCL) to acquire the essential electrical facts for each of the diodes in the circuit. Sometimes the electrical facts are simple, i.e. that the current through the diode = 0 because the diode is in reverse bias.

Emphasis needs to be made that the art of inspection is vital to analysis of circuits that include diodes. More diodes require more inspection. Inspection identifies the allowed and disallowed diode states. Consider the example of a string of diodes as represented by example 9.3-4:

EXAMPLE 9.3-5: Determine node voltages V_1, V_2. V_3, V_4 and the currents through each of the diodes for $R_1 = 4.0$, $R_2 = 2.5$, $R_3 = 2.5$ and $R_4 = 5.0$ (all in kΩ). Assume the CVD model.

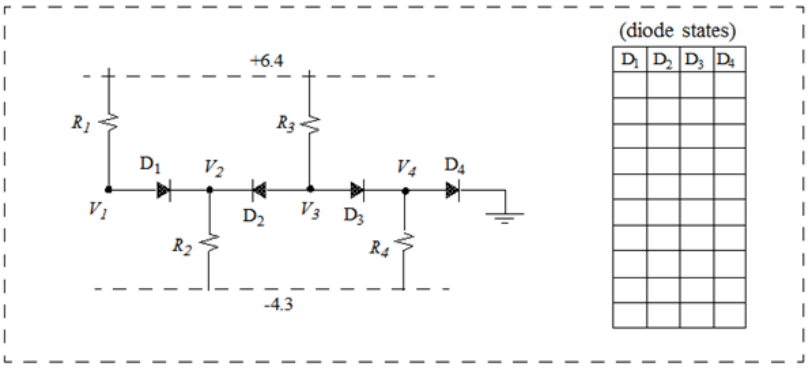


Figure E9.3-5: Diode string

SOLUTION: Notice that we have included a 'state table' for all of the possible diode states. But just like the previous example it may be assured that some diodes have no choice. For example diode D_1 must always be ON since the current through R_1 has to go somewhere and the diode is correctly oriented for it to do so.

The rest of the possible options are shown by the completed state table. Note that D_3 must also always be on (why?).

(diode states)

D_1	D_2	D_3	D_4
1	1	1	1
1	1	1	0
1	0	1	1
1	0	1	0

Only one of these states is valid. So we pick one and try it out. The rule is (always) '<u>simplest first</u>'. And the [1 1 1 1] state is the most likely candidate since it allows all node voltages be identified by stepping from right to left, beginning with D_4:

i.e. $V_4 = 0.7$V, $V_3 = 1.4$V, $V_2 = 0.7$V, $V_1 = 1.4$V

from which we obtain (by inspection) $I_1 = 1.25\text{mA}$, $I_2 = 2.0\text{mA}$, $I_3 = 2.0\text{mA}$ and $I_4 = 1.0\text{mA}$.

and for which (1) $I_{D1} = I_1 = 1.25\text{mA}$
(2) $I_{D2} = I_2 - I_{D1} = 0.75\text{mA}$
(3) $I_{D3} = I_3 - I_{D2} = 1.25\text{mA}$
And (4) $I_{D4} = I_{D3} - I_4 = 0.25\text{mA}$

Since all of these are positive then the assumption that all diode are in a conducting state is true and hence

$V_4 = \mathbf{0.7V}$, $V_3 = \mathbf{1.4V}$, $V_2 = \mathbf{0.7V}$, $V_1 = \mathbf{1.4V}$

$I_{D1} = \mathbf{1.25mA}$, $I_{D2} = \mathbf{0.75mA}$, $I_{D3} = \mathbf{1.25mA}$, $I_{D4} = \mathbf{0.25mA}$

Notice that we do not highlight the answers until they are confirmed.

Because diodes have two state (ON, OFF) their analysis becomes a binary set of possible states. In this case it should be clear that some states cannot possibly exist and there is no point in pursuing them. And once again the process of analyzing diode circuits needs to use *inspection* to identify what states can exist and are worth a pursuit.

Note that the engineer (or his software) has to undertake this sorting process and identify the possible allowed diode states before invoking any mathematics. Otherwise he/she is just spitting into the wind.

The rest of the story is that there were still a handful of possible states left. Be assured that only one state can be true, and so the 'art' of electronics is to choose wisely. But have no cause to fear. The art is straightforward and always follows the rule: 'Try the simplest one first'

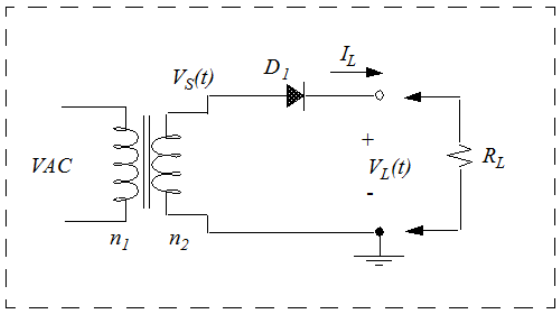
Even so, we have to realize that the simplest possibility may not be the 'lucky' correct one, as was the case for this example.

In fact were resistance $R_4 = 2.5\text{k}\Omega$ in exercise 9.3-5, then the value of $I_{D4} = -0.75\text{mA}$, which is impossible. And so in that case the simplest state would not be valid. Therefore it would be necessary to test the next simplest case, whichever one that might be.

In exercise 9.3-5 the next simplest state would probably be the one for which $(D_1,D_2,D_3,D_4) = [1\ 0\ 1\ 0]$ since it is merely two separated diode strings.

9.4 DIODE RECTIFIERS CIRCUITS and AC-DC CONVERTERS

One of the earliest usages of the diode was energy conversion, specifically AC- to –DC. Early in the history of the power grids it became evident (via the War of Currents) that alternating voltages were the best way to transmit power over distance, whereas the best form of locally useful energy was a fixed voltage source supplying a direct current (DC). Most electronic circuits use a single pole (DC) polarity in the form of voltage rails. So for a distribution system that uses an AC grid, the diode component is made to order for the AC-DC conversion, whether it be a vacuum diode or a *pn* junction. The concept is shown by figure 9.4-1.



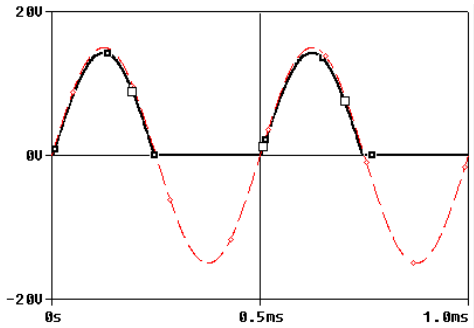


Figure 9.4-1(a). Series diode and load, also called a half-wave rectifier (HWR). When Vs < 0 the current flow is blocked by the 'OFF' state of the diode.

Figure 9.4-1(b). Voltage across the load due to I_L. A resistance load is always elected because it is a dissipative element.

The average voltage for figure 9.4-1(b) is

$$\langle V_L(t)\rangle = \frac{1}{T}\int_0^T V(t)dt = V_L \times \frac{1}{2\pi}\left[\int_0^{\pi}\sin(\theta)d\theta + \int_{\pi}^{2\pi} 0 d\theta\right] \qquad = \frac{1}{\pi}\times V_L \qquad (9.4\text{-}1)$$

and the average power delivered to the load is

$$\langle P_L(t)\rangle = \frac{1}{\pi^2}\times\frac{V_L^2}{R_L} \qquad \cong 0.1\frac{V_L^2}{R_L} \qquad (9.4\text{-}2)$$

It is always in order to include a transformer input coupling as shown by figure 9.4-1(a) both for (1) isolation and for (2) control of the voltage amplitude at the secondary = V_S. If V_S is less than 10V it is in order to include a diode drop, even though accuracy is not that critical in the art of electronics.

The rest of the story is that there is another quick AC-DC option using four diodes (affectionally called a diode bridge) as shown by figure 9.4-2(a).

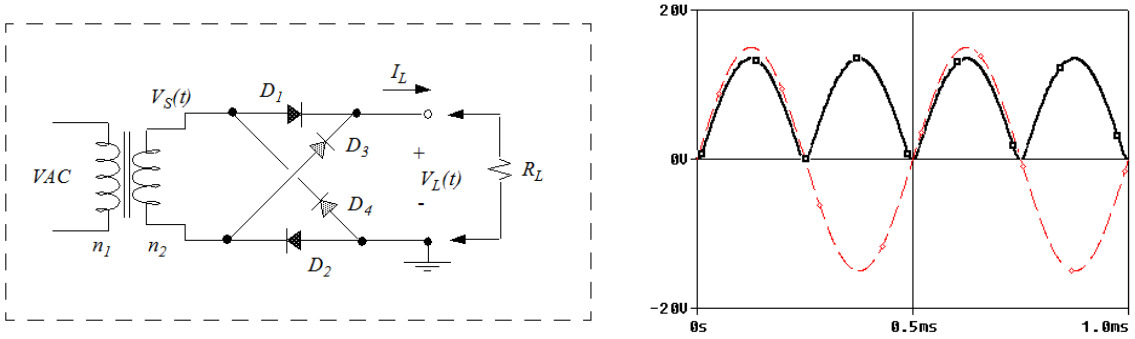


Figure 9.4-2(a). Diode bridge and load, also called a full-wave rectifier (FWR).
Figure 9.4-2(b). Voltage across the load due to current through the diodes for the FWR (a.k.a. FWB).

Note that the contribution to I_L comes from both polarities (1) the conductive loop through D1 and D2 formed when Vs > 0 and (2) the conductive loop through D3 and D4 when Vs < 0. The outcome is shown by Figure 9.4-2(b)

The FWR topology may also be drawn in bridge form shown by figure 9.4-5.

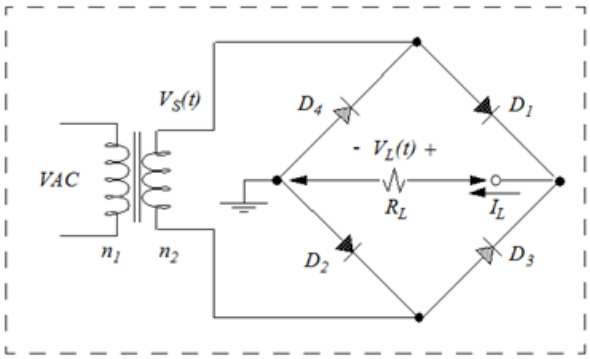


Figure 9.4-3 Full-wave rectifier (FWR) topology of figure 9.4-2(a) drawn as a full-wave bridge (FWB). Compare the position of the diodes between this figure and that of figure 9.4-2(a)

And the same mathematics applies to the FWR as equation (9.4-1) except there are two half waves that add up to give a factor of two

$$\langle V_L(t)\rangle = \frac{2}{\pi}\times V_L \qquad (9.4\text{-}3)$$

for which the average power delivered to the load is

$$\langle P_L(t)\rangle = \frac{4}{\pi^2}\times\frac{V_L^2}{R_L} \cong 0.4\frac{V_L^2}{R_L} \qquad (9.4\text{-}4)$$

Average current through R_L identifies one-one with the count of rectified half-waves. So if the source is three-phase (3ϕ) then the count of half-waves across R_L is three and the current is of the form represented by figure 9.4-4.

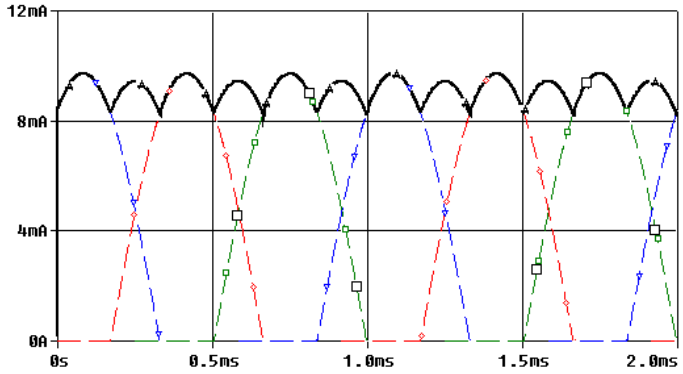


Figure 9.4-4. Three-phase sum of rectified currents. The outcome shows up as a steady-state signal with a ripple of peak-peak amplitude V_R and frequency = $6 \times f_0$.

The averaged output level for the 3ϕ rectifier is then

$$\langle V_L(t) \rangle = \frac{3}{\pi} \times V_L \tag{9.4-5}$$

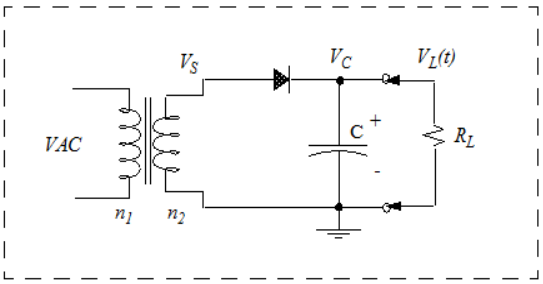
and the power to the load is

$$\langle P_L(t) \rangle = \frac{9}{\pi^2} \times \frac{V_L^2}{R_L} \cong 0.91 \frac{V_L^2}{R_L} \tag{9.4-6}$$

The output voltage level V_L, as well as being close to unity, is also one for which the ripple is small and mathematically of the value

$$\Delta V_L = 0.134 \times V_L = V_R \tag{9.4-7}$$

Equations (9.4-5) through (9.4-7) point out an aspect of the AC-DC converter that is of importance, namely an output that is as much like an ideal voltage rail as possible. Ripple V_R needs to be small, and that invites the use of a few modifications to single-phase AC-DC converters, as represented by figures 9.4-5(a) and 9.4-5(b)



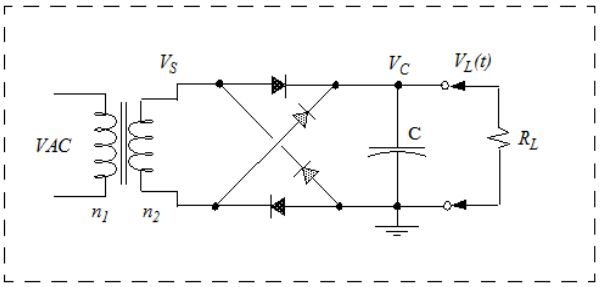
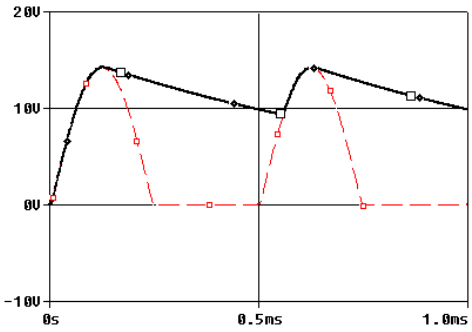


Figure 9.4-5(a) HWR with a capacitance in parallel with the load
Figure 9.4-5(b) FWR with a capacitance in parallel with the load



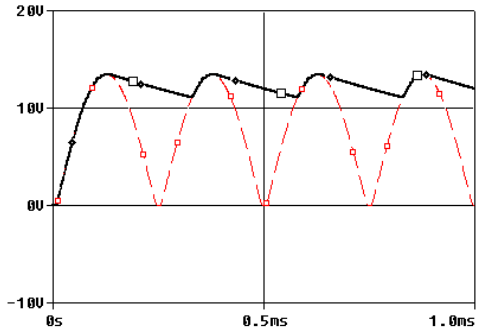


Figure 9.4-6(a) HWR output with C

Figure 9.4-6(b) FWR output with C

The effect of the capacitance is to store charge at whatever voltage it is supplied. The relaxation of the stored charge as it discharges through the load R_L is represented by

$$V_C(t) = V_P e^{-t/\tau} \qquad (9.4\text{-}8)$$

where $\tau = R_L C$ and

$$t \cong T_{\text{period}} = 1/f \quad \text{if HWR} \qquad (9.4\text{-}9a)$$
$$t \cong T_{\text{period}} = 0.5/f \quad \text{if FWR} \qquad (9.4\text{-}9b)$$

From figure 9.4-5 it should be evident that these are very rough approximations. But this subject area is electronics, not accounting.

The corresponding ripples are then

$$V_R = V_P - V_P e^{-t/\tau} \approx V_P / fRC \quad \text{if HWR} \qquad (9.4\text{-}10a)$$
$$\approx 0.5 V_P / fRC \quad \text{if FWR} \qquad (9.4\text{-}10b)$$

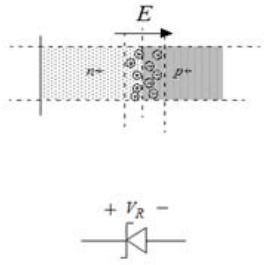
where V_P is the peak voltage across the capacitance, sometimes also called V_C for emphasis

and is $V_P = V_S - V_D$ for HWR (9.4-11a)

$V_P = V_S - 2V_D$ for FWR (9.4-11b)

And $\langle V_L(t) \rangle \cong V_P - 0.5V_R$ (9.4-12)

In spite of this exposition, it is more likely that the fat knobs that resemble a wall plug do not pause at one of the above options. Most of the time they will contain an extra diode that will almost ensure that the output is flat. This diode component is called a Zener diode, so named after the Zener breakdown effect (Clarence M. Zener) which occurs when the junction is alloyed with heavy doping on both sides so that the built-in E-field is close to the breakdown limit. A typical I-V response is shown by figure 9.4-7(b)



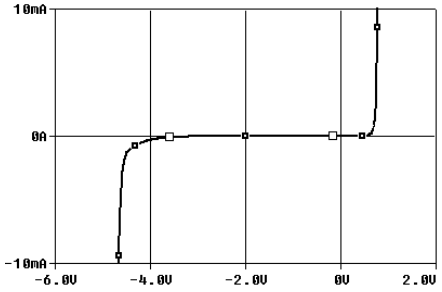


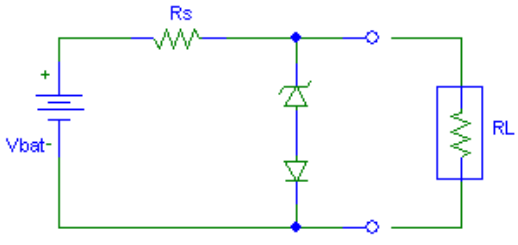
Figure 9.4-7(a) Zener diode component. When V_R exceeds V_Z the junction breaks down.
Figure 9.4-7(b) Zener diode I-V response (spice rendition of 1n750, V_Z = 4.3V zener diode.

By adjustment of the doping levels, zener breakdown voltages from 1.8V to 90V are not uncommon.

The selection of breakdown voltages provides a ready candidate for regulation of the voltage level. Zener diodes with V_Z > 5.0V have a positive temperature coefficient on the order of +3mV/°C (although it varies with V_Z) , so it usually is placed in series with a forward-biased junction diode as is indicated by the figure. The temperature coefficient for the diode junction is typically on the order of -3mV/°C, and so the effects will cancel and the output will be reasonably well-behaved over a large range of current variations.

A typical Zener application is represented by example 9.4-1.

EXAMPLE 9.4-1: The circuit shown represents a simple automotive voltage-reduction circuit with a variable source 12 < *Vbat* < 15V and a 300mW load that may either be ON or OFF. The Zener diode is a 1n754 (V_Z = 6.8V) and the junction diode has forward voltage drop V_D = 0.7V.



Find: (a) drop-down resistance R_S such that the Zener diode set always remains in reverse breakdown (maintains regulation) with current minimum of 5 mA and (b) (1) the worst-case power dissipated in the Zener diode and (2) in the resistance *Rs*.

SOLUTION: The voltage across the load is $V_L = V_Z + V_D$ $= 6.8 + 0.7$ $= 7.5\text{V}$
So the current drawn by the application is $I_L = P_L/V_L$ $= 300\text{mW}/7.5\text{V}$ $= 40\text{mA}$

Therefore the minimum current that must be supplied by the source

$= I_L + I_Z(min)$ $= 40\text{mA} + 5\text{mA}$ $= 45\text{mA}$

Vbat(min) must be able to supply 45mA through R_S , which must then be

$R_S = [Vbat(min) - V_L]/I_S(min)$ $= (12 - 7.5)/45\text{mA}$ $= 0.1\ \text{k}\Omega$ $= \mathbf{100\Omega}$

The worst-case power dissipated through the Zener diode is when Vbat = Vbat(max) and the load is OFF.

The current that flows through R_S will be $I_S(max) = (15 - 7.5)/0.1\text{k}\Omega = 75\ \text{mA}$

All of this current will flow through the Zener diode when the application is OFF and therefore

$P_L(worst) = 6.8\text{V} \times 75\text{mA} = 510\text{mW} = \mathbf{0.51W}$

Take note from the example that the Zener diode must always have a drop-down resistance, both because it is required that $V_Z < V(source)$ and because the R_S is needed to limit the current through the zener diode.

This context is represented in a more typical use of a Zener diode in context with an AC-DC converter topology as shown by example 9.4-2

EXAMPLE 9.4-2: For the FWR topology shown choose component values that will support a Zener regulated 240mW, 6V application from a 120V 60Hz power tap. Transformer turns ratio $n_{12} = 12{:}1$. Assume all diode are Si power diodes ($V_D = 0.8\text{V}$)

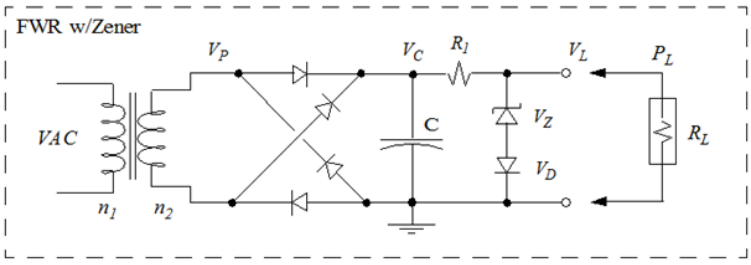


Figure E9.4-2 Full-wave rectifier AC-DC Zener-regulated charging plug.

(a) Determine V_C and V_P

(b) If $V_C(min) = 8.0V$ with the load connected, what values of R_1 and C_1 are required, assuming that the current through the Zener diode approaches zero when V_C approaches $V_C(min)$.

(c) What average power must the Zener diode dissipate when the load is not connected?

SOLUTION:

(a) Since 120V is rms then $V_P = \sqrt{2} \times V_{rms} \times \frac{n_1}{n_2} = \sqrt{2} \times 120 \times \frac{1}{12}$ = **14.1V**

and $V_C = V_P - 2 \times V_D$ = 14.1 – 2 x 0.8 = **12.5V**

The characteristics of the load are P_L = 240 mW at 6.0V,

so I_L = 240mW/6.0 = 40 ma and R_L = 6.0V/40mA = 150Ω

and from the requirement that $V_C(min)$ be able to provide $I_L + I_Z(min)$ = 40mA + 0, then R_S will be

$R_S = [V_C(min) - V_L]/I_S(min)$ = (8.0 – 6.0)/40mA = **50Ω**

Since the ripple $V_R = [V_C(max) - V_C(min)]$ = 12.5 – 8 = 4.5V and the resistance load to the capacitance

$R = R_S + R_L$ = 150 + 50 = 200Ω

Then, from equation (9.4-10b) $C \approx 0.5(V_C/V_R)/fR$ = $0.5(12.5/4.5)/(60 \times 200)$ = **116μF**

The power dissipated in the Zener diode when the load is not connected is an average between the situation for which V_C = 12.5V and V_C = 8.0V. When V_C = 8.0V then $I_Z = I_L$ (= I_S (*min*)) = 40mA since in the absence of a load all of the current must go through the Zener. When V_C = 12.5V then the current through the drop-down resistance R_S will be

$Is(max) = [V_C(max) - V_L]/R_S$ = [12.5 – 6.0]/50Ω = 130 mA

The average current that the zener diode must accommodate = $[I_S(max) + I_S(min)]/2$. Since the Zener diode is in series with a junction diode then the Zener voltage has to be

$V_Z = V_L - V_D$ = 6.0 – 0.8 = 5.2V

and so the averaged power that it must be able to accommodate is

$\langle P_Z(t) \rangle \cong V_Z \times [I_S(\max) + I_S(\min)]/2$ = 5.2 × [130 + 40]/2 = **442mW**

If you held the patent on the circuit topology used in example 9.4-2 you could probably claim royalties of about 10 cents on each instance, regardless of their external shape. At least 20% of the people on the planet, to include children, have at least one of these circuits associated with their cell phone, laptop, or toy. They probably also buy a new one every year. There are about 6B people in the world

So the patent holder could claim a royalty stream of $\$.10 \times 20\% \times 6B / yr = \$120M/yr.$

Unfortunately the patent on this topology has long expired. But this sort of circuit construct and patent analysis is what engineers are tasked to do.

9.5 DIODE-CAPACITANCE CIRCUITS

The most interesting circuits in the diode kingdom are those in which a capacitance is involved. That might seem a little strange since there are only two basic circuits, one of which is the peak detector, shown by figure 9.5-1.

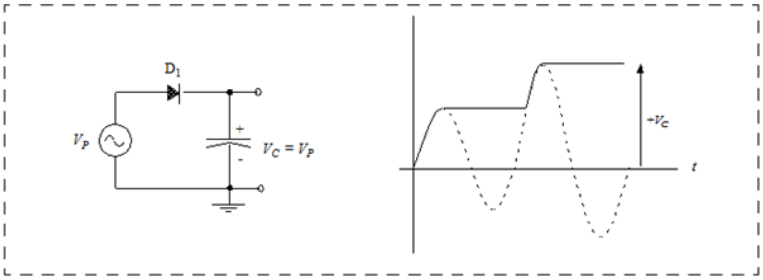


Figure 9.5-1. Peak detector

And the other of which is the level-shifter, shown by figure 9.5-2.

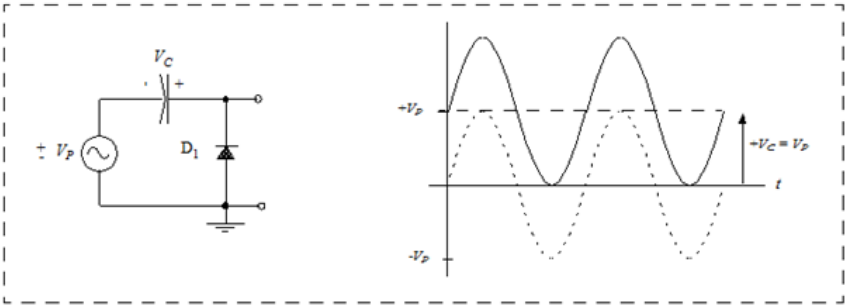


Figure 9.5-2. level shifter

The peak detector captures the peak. And if the source is sinusoidal, as in the previous section, it will capture the peak voltage and hold it as charge stored on the capacitance. If a load is included as in figure 9.4-5(a) the charge will discharge through the load until it is renewed by the next peak.

The level shifter does rely on the input signal being bipolar, as indicated by figure 9.5-1(b). Since there is no way for the capacitance to discharge, it captures voltage V_C = (either $+V_P$ or $-V_P$) across the capacitance. So the output is shifted relative to the input by the voltage captured across C.
But notice that we can use a peak detector as a next stage to a level shifter, as shown by figure 9.5-3.

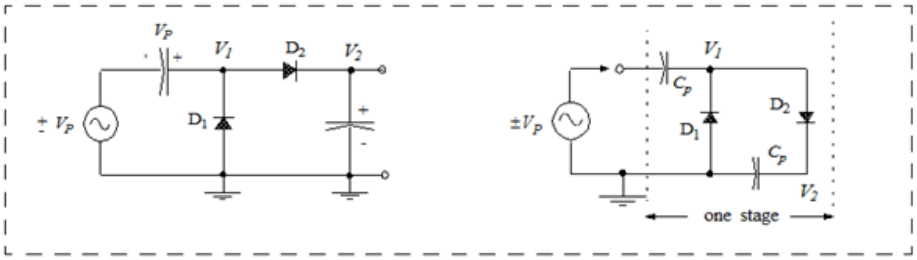


Figure 9.5-3. level shifter followed by peak detector. This becomes an AC-DC converter with $V_L = 2(V_P - V_D)$ (and ripple). This circuit topology is sometimes called a voltage doubler.

If we do a little topology adjustment the voltage double becomes a stage in a series of voltage doublers, with the peak becoming progressively higher as shown by figure 9.5-4.

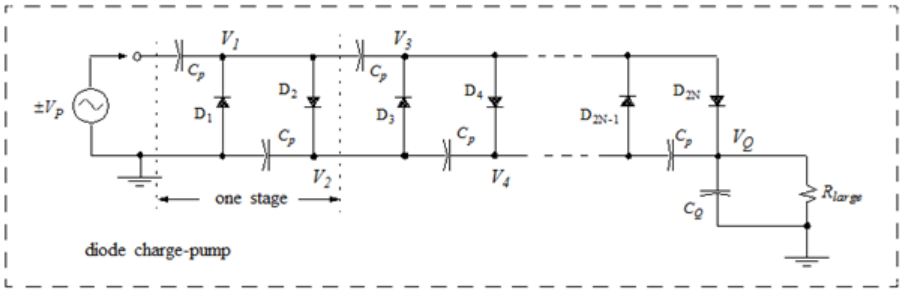


Figure 9.5-4. Cockroft-Walton voltage multiplier (a.k.a charge pump)

For the charge pump the output voltage is

$$V_Q = 2N \times (V_P - V_D) \qquad (9.5\text{-}1)$$

Where N = number of stages. If a load is included the charge-pump circuit could also be identified as an AC-DC multiplier converter. A pspice rendition of a four-stage charge pump is shown by figure 9.5-5.

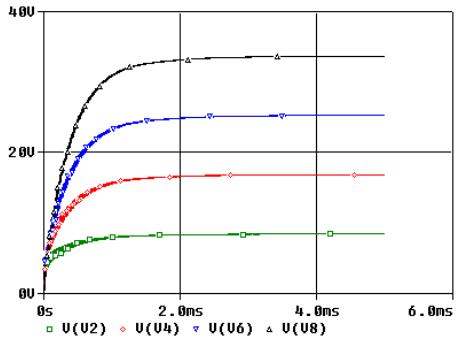


Figure 9.5-5. Pspice rendition of 4-stage charge pump. The successive nodes voltages are shown.

As a boost AC-DC converter the charging cycle limits its current flow. At maximum charge transfer this corresponds to maximum current

$$I_Q = \Delta Q/dt \qquad = 2C_P\,(V_P - V_D) \times f \tag{9.5-2}$$

The diode charge pump supports an AC-DC boost supply but only for a small number of stages. It primarily is used to store a large voltage on a storage capacitance as shown for use in electrostatic applications such as X-ray systems, air ionizers, copy machines, and bug zappers.

Each stage can, at most, only push a small increment of charge energy forward

$$w(\text{ea}) = 2 \times [\tfrac{1}{2}\, C_P\, (2V_P)^2] \tag{9.5-3}$$

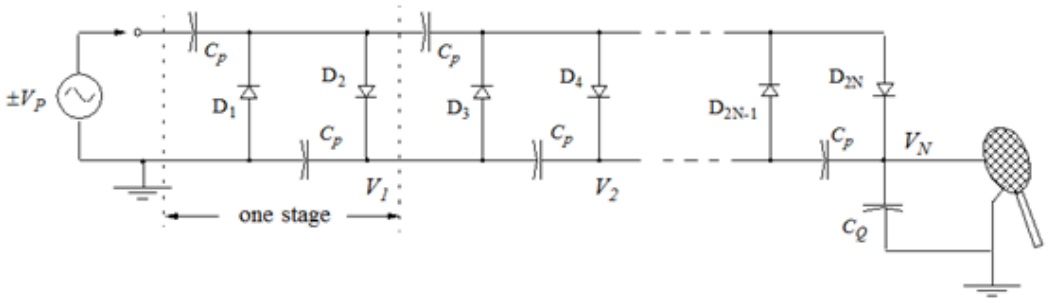
and the storage capacitance C_Q stores energy

$$W_Q = \tfrac{1}{2} C_Q\, V_N^2 \qquad = 2C_Q\, N^2 V_P^2 \tag{9.5-4}$$

And so the number of cycles required to charge the capacitance to its maximum level is

$$n = W_Q/w(ea) \quad = N^2 C_Q/2C_P \tag{9.5-5}$$

EXAMPLE 9.5-1: The charge pump circuit shown is to be used to drive an electrostatic tennis racquet used to swat and electrocute mosquitoes. Assume that the grid wires are 0.2mm apart and the electrostatic field must be kept less than ½ of the breakdown field of air (30kV/cm). Input signal amplitude V_P = 2.2V. The pump capacitances C_p = 50pF each and the storage capacitance C_Q = .01μF.



Assume Si (V_D = 0.7V) model for the diodes
An integrated circuit is to be constructed. Determine the following

(a) Voltage V_N needed to electrocute mosquito.
(b) Number of stages needed to achieve V_N (= V_Q).
(c) What energy W_Q is released by C_Q on discharge?
(d) Assume signal frequency 12.5MHz. If the energy held by each stage contributes incrementally to the energy W_Q stored on C_Q, how long will it take to reach V_N .?

SOLUTION: V_N needed to achieve ½ × (30kV/cm) is V_N = 15kV/cm × 0.02cm = **300V**

The voltage achieved across each stage = $V_C = 2(V_P - V_D)$ = 2(2.2 – 0.7) = 3.0V

And therefore the number of stages needed is $N = V_Q/V_C$ = **100 stages**

The energy released on discharge is $W_Q = ½ \times C_Q V_Q^2$ = 0.5 × .01μF × 300^2 = **0.45mJ**

The number of cycles to charge up capacitance C_Q is

$$n = N^2 C_Q/2C_P = 100^2 \times .01\mu F/(2 \times 50pF) = 10^6$$

and so the time it takes to charge up the capacitance is

$$T = \Delta t \times n = (1/f) \times n = 10^6/12.5MHz = \mathbf{0.08\ s}$$

The level shifter topology of figure 9.5-2 can be made considerably more flexible as is shown by figure 9.5-6

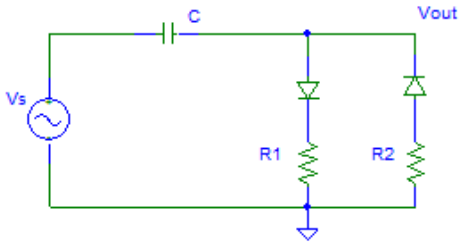


Figure 9.5-6. Adjustable level shifter

If *Vs* is a square wave and the *RC* time constants are long, then the output is reasonably stable and has relatively little sag, as represented by figure 9.5-7

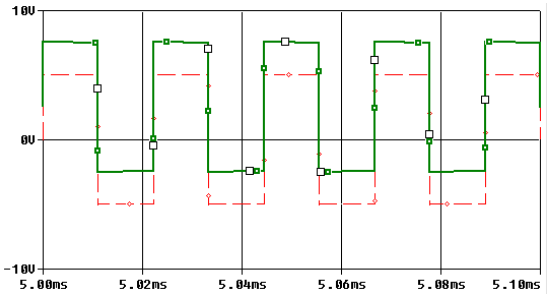


Figure 9.5-7. Adjustable level shifter, square-wave input. The input square wave is the dashed trace, 5V amplitude. R_1 = 40kΩ, R_2 = 10 kΩ, C = .02μF and f = 45kHz.

For a square-wave output the new output levels will be V_1 and $-V_2$. At equilibrium the quantity of charge added and subtracted to the capacitance must balance, i.e. $\Delta Q^+ = \Delta Q^-$, where

$$\Delta Q^{+} = \int_{0}^{T_P} I_2 dt = \frac{|V_2| - V_D}{R_2} T_P \qquad (9.5\text{-}6a)$$

$$\Delta Q^{-} = \int_{T_P}^{2T_P} I_1 dt = \frac{|V_1| - V_D}{R_1} T_P \qquad (9.5\text{-}6b)$$

And so

$$\frac{|V_2| - V_D}{|V_1| - V_D} = \frac{R_2}{R_1} \equiv \alpha_{21} \qquad (9.5\text{-}7)$$

Where V_D = diode drop. And since $|V_1| + |V_2| = 2V_P$, with V_P = peak of the input square wave then

$$|V_1| - V_D = 2(V_P - V_D)/(1 + \alpha_{21}) \qquad (9.5\text{-}8)$$

Which is the same as $|V_1| = 2(V_P - V_D)/(1 + \alpha_{21}) + V_D$

And then the shift in the output ΔV is

$$\Delta V = |V_1| - V_P = 2(V_P - V_D)/(1 + \alpha_{21}) - (V_P - V_D) \qquad (9.5\text{-}9)$$

$$\Delta V = (V_P - V_D) \times \frac{(1 - \alpha_{21})}{(1 + \alpha_{21})} \qquad (9.5\text{-}10)$$

EXAMPLE 9.5-2: For an input square wave of V_P = 5V amplitude, R_1 = 40kΩ, R_2 = 10 kΩ, determine the level shift assuming that the capacitance is large enough to avoid sag in the waveforms for the frequency of interest. Assume V_D = 0.7V.

SOLUTION: a_{21} = 10k/40k = 0.25

And by equation (9.5-10) $\Delta V = (5 - 0.7) \times \frac{(1 - 0.25)}{(1 + 0.25)}$ = **2.53 V**

Example 9.5-2 and figure 9.5-7 make use of the same component values and the ΔV shift indicated by figure 9.5-7 is consistent with the numerical result of example 9.5-2.

The shift is also dependent on the waveform, as may be illustrated by the option for which V_S is a triangular waveform as shown by figure 9.5-8.

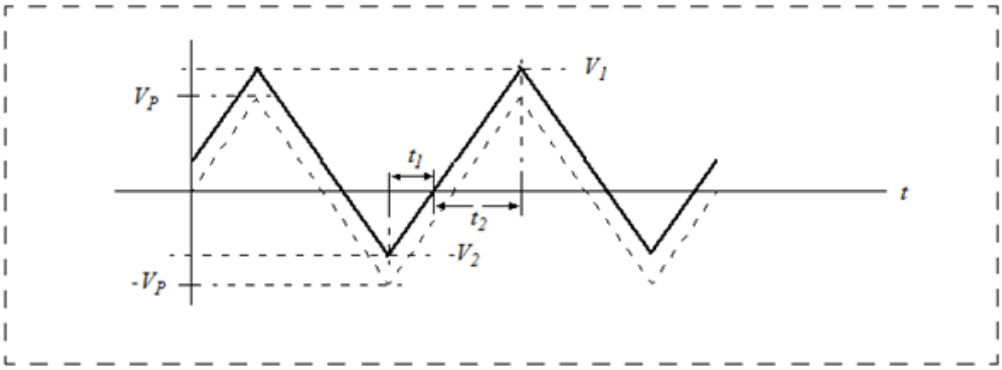


Figure 9.5-8. Adjustable level shifter, triangular-wave input representation.

Equations (9.5-6a) and (9.5-6b) then become

$$\Delta Q^{+} = \int_{0}^{2t_1} I_2 dt = \frac{|V_2| - V_D}{R_2} \times 2t_1 \tag{9.5-11a}$$

$$\Delta Q^{-} = \int_{0}^{2t_2} I_2 dt = \frac{|V_1| - V_D}{R_1} \times 2t_2 \tag{9.5-11b}$$

For which the balance, i.e. $\Delta Q^{+} = \Delta Q^{-}$ gives

$$\frac{|V_2| - V_D}{|V_1| - V_D} \times \frac{t_1}{t_2} = \frac{R_2}{R_1} \tag{9.5-12}$$

But from figure 9.5-8 and the similar triangles

$$\frac{t_1}{t_2} = \frac{V_2}{V_1} \tag{9.5-13}$$

When this is translated into the current pushed by V_1 and V_2 through the diode for which V_1 would be replaced by $V_1 - V_D$ and V_2 would be replaced by $V_2 - V_D$ then

$$\left(\frac{|V_2| - V_D}{|V_1| - V_D} \right)^2 = \frac{R_2}{R_1} \tag{9.5-14}$$

or $$\frac{|V_2|-V_D}{|V_1|-V_D}=\alpha_{21} \qquad (9.5\text{-}15a)$$

with $$\alpha_{21}=\left(\frac{R_2}{R_1}\right)^{1/2} \qquad (9.5\text{-}15b)$$

Equation (9.5-15a) is syntactically the same as equation (9.5-7). So the outcome is the same, i.e. equation (9.5-10) is also valid for the triangular waveform but with α_{21} given by equation (9.5-15b).

In like manner other waveforms can be assessed. For the sinusoidal wave the approximation of a parabolic form in (t_1/t_2) may be assumed for which (9.5-14) would become

$$\left(\frac{|V_2|-V_D}{|V_1|-V_D}\right)^{3/2}=\frac{R_2}{R_1} \qquad (9.5\text{-}16a)$$

with $$\alpha_{21}=\left(\frac{R_2}{R_1}\right)^{2/3} \qquad (9.5\text{-}15b)$$

For comparison to the previous example consider example 9.5-3 with the same construct but with a sinusoidal form.

EXAMPLE 9.5-3: For an input sinusoidal wave of V_P = 5V amplitude, R_1 = 40kΩ, R_2 = 10kΩ, determine the level shift assuming sufficiently large time constants so that the equilibrium conditions will be true. Assume V_D = 0.7V.

SOLUTION: $$\alpha_{21}=\left(\frac{10k}{40k}\right)^{2/3} = 0.397$$

And by equation (9.5-10) $$\Delta V=(5-0.7)\times\frac{(1-0.397)}{(1+0.397)} = \underline{\mathbf{1.86\ V}}$$

The results are shown by figure E9.5-2.

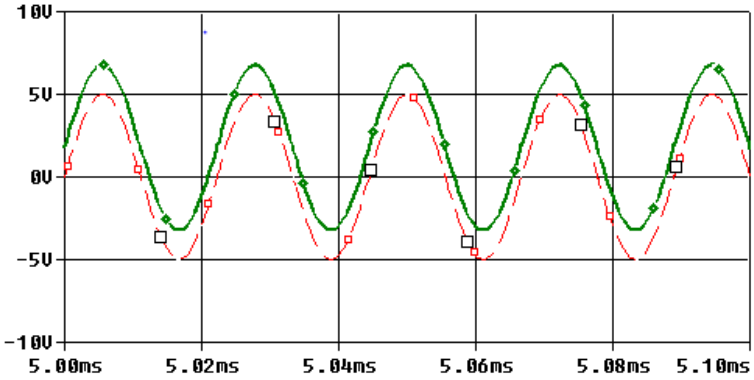


Figure E9.5-2: Adjustable level shifter, sinusoidal input, simulations results. The input is the dashed trace, 5V amplitude. R_1 = 40kΩ, R_2 = 10 kΩ, C = .02μF and f = 45kHz.

Compare figure E9.5-2 to figure 9.5-7 and take note that the shift ΔV is slightly less than for the square wave as well as being consistent with the result above.

9.6 WAVE-SHAPING TOPOLOGIES

As has been outlined in previous chapters, the greater majority of circuits are two-port networks for which an input waveform is transferred from input port to output port through a circuit construct. If the circuit construct uses only linear components then the output is an exact copy of the input, with the slope (= dV_{out}/dV_{in}) forming a multiplying factor. For a circuit that contains only linear components the slope is a constant and always of value ≤ 1.0.

But a circuit that contains diodes introduces a non-linear element to the transfer ratio. Fortunately, with diodes the non-linearity shows up primarily as breakpoints in the transfer curve. Consider the circuit shown by figure 9.6-1a.

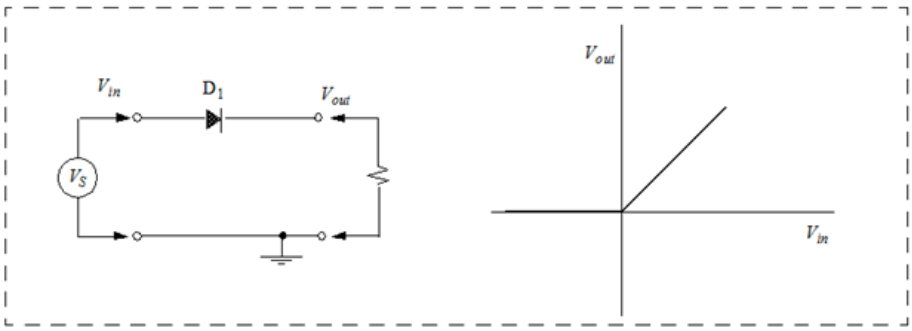


Figure 9.6-1a. Simple wave-shaping circuit using a single diode.

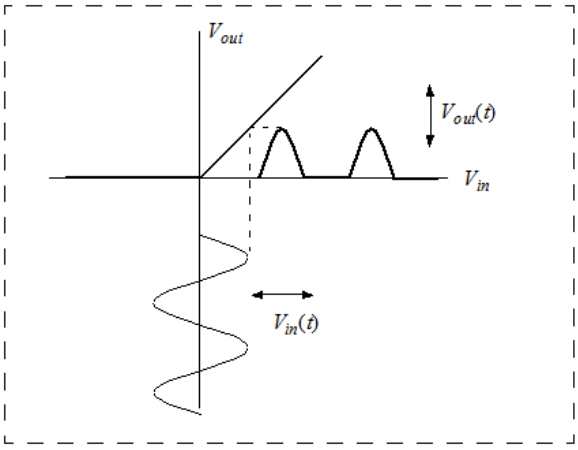


Figure 9.6-1b. Sinusoidal signal transfer for the transfer curve of figure 9.6-1a

You already know of this circuit as that of the half-wave rectifier topology. The transfer curve is a consequence of a breakpoint at $V_{in} = 0$. For $V_{in}(t) < 0$ the slope $dV_{out}/dV_{in} = 0$, which also correspond to the 'OFF' state of the diode. For $V_{in}(t) > 0$ the slope $dV_{out}/dV_{in} = 1$ and the V_{out} is a copy of the input.

The Zener diode also serves as a means to achieve breakpoints, usually at higher bias voltages as illustrated by figures 9.6-2a and 9.6-2b.

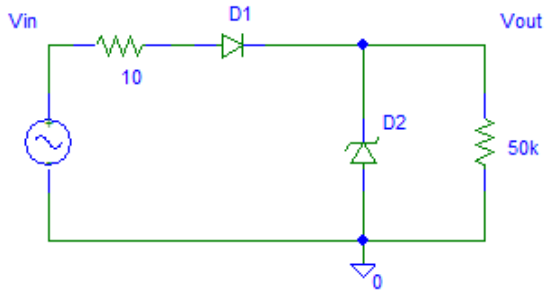


Figure 9.6-2a. Modification of figure 9.6-1a to include a 1n750 Zener diode ($V_Z = 4.7$V).

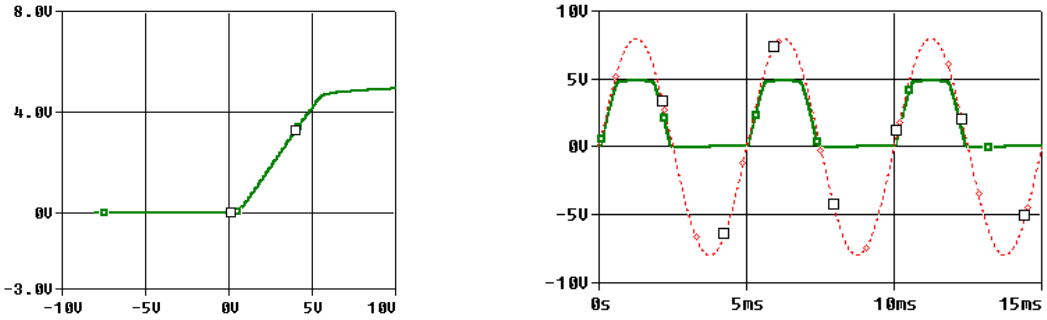


Figure 9.6-2b. Pspice rendition of figure 9.6-2a, showing (1) transfer curve and (2) V_{out} result for sinusoidal input with $V_P = 8.0$V. The resulting output waveform is (roughly) a set of trapezoidal pulses.

If one waveform is shaped from another then the two dissimilar waveforms will automatically be coherent. This is represented by example 9.6-1

EXAMPLE 9.6-1: Use a wave-shaping network to reshape a triangular-wave input to a sinusoidal form using a diode-waveshaping network.

SOLUTION: Since the output must be shaped for both polarities of the input waveform a full-wave option is necessary as represented by figure E9.6-1

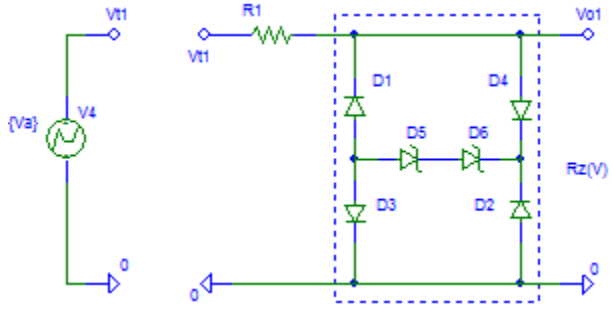


Figure E9.6-1a. Use of diode bridge with in750 Zener diodes to create a clipper breakpoint at approximately 10.0 V.

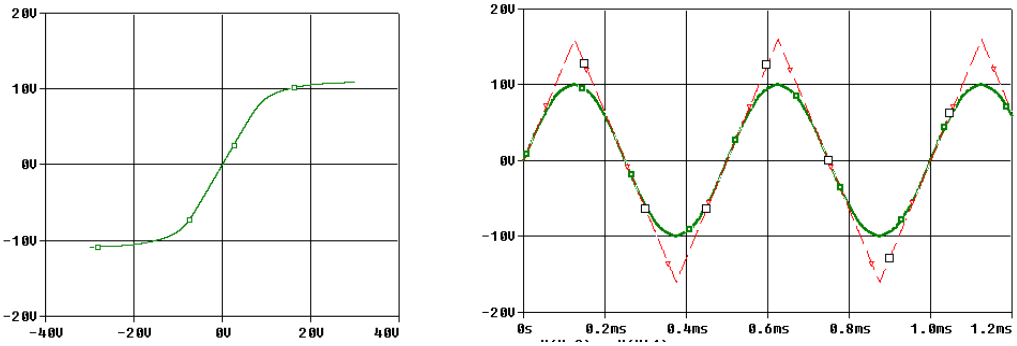


Figure E9.6-1b. pspice rendition of (1) waveshaping transfer curve (2) output waveform as shaped from triangular-wave input.

Note that the construct essentially forms a simple voltage divider with

$$\frac{V_{OUT}}{V_{IN}} = \frac{Rz(V)}{R_1 + Rz(V)} \qquad \text{(E9.6-1)}$$

and for $V < V_{break}$, $Rz(V) = \infty$ and consequently the ratio = 1.0 (and slope = 1.0).

The output result is also a consequence of an informed choice of amplitudes for (1) the triangular wave input and (2) the resulting sinusoidal output. This amplitude is predicated on the context that both waveforms should have the same slope at $t = 0$.

For the triangular waveform

$$\left.\frac{dV}{dt}\right|_{t=0} = \frac{V_T}{(T/4)} = 4fV_T \qquad = 4fV_T \qquad \text{(E9.6-1)}$$

and for the sinusoidal waveform

$$\left.\frac{dV}{dt}\right|_{t=0} = \frac{d}{dt}\left[V_P \sin(\omega t)\right] = \omega V_P \cos(\omega t)\Big|_{t=0} \qquad = 2\pi f V_P \qquad \text{(E9.6-2)}$$

For these slopes to be equal then it is therefore necessary that

$$\frac{V_T}{V_P} = \frac{\pi}{2} \qquad \text{(E9.6-3)}$$

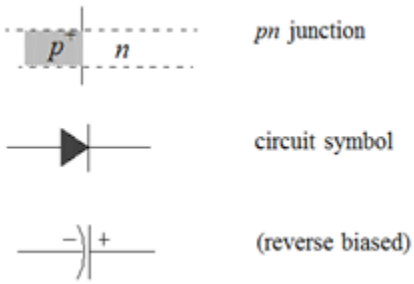
For the two 1n750 diodes in series with the generic (= 1n914) diodes the peak voltage V_{P0} is approximately 10.0 and so the required amplitude for the triangular wave is

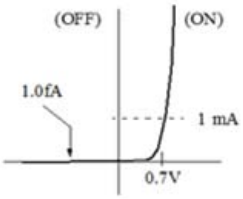
$$V_T = \frac{\pi}{2} \times V_P \qquad = \underline{\mathbf{15.7\ V}}$$

The options on wave shaping circuits are a matter of choice. For passive circuit components as have been represented heretofore there are innumerable options, all of which will form breakpoints from one slope to another, with the caveat that all slopes are ≤ 1.0. If active elements (e.g. opamps, transistors) are included then transfer slopes > 1.0 are also feasible, but are subject to constraints imposed by power supply rails and by the non-linearities of the active elements (transistor set).

PORTFOLIO and SUMMARY

(a) *pn* junction





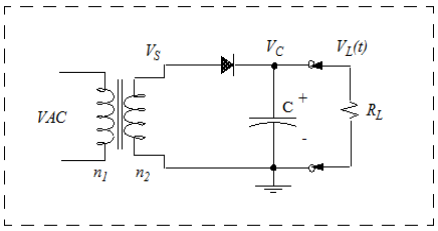
$$I \cong I_S\left(e^{V/nV_T} - 1\right)$$

$$V_T = kT/q \cong .025V$$

$\Delta V_D \cong 60mV$ for each decade increase in current

$$C_J = C_{J0}/\left[1 + V_R/\varphi_J\right]^{MJ}$$

(b) AC-DC converters



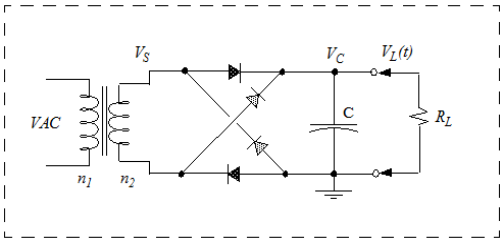
$V_P = V_S - V_D$ for HWR

$V_P = V_S - 2V_D$ for FWR

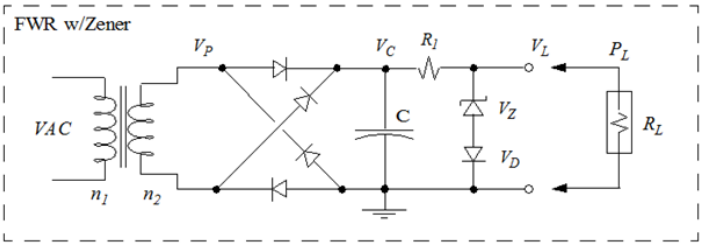
$V_R \approx V_P / fRC$ if HWR

$\approx 0.5V_P / fRC$ if FWR

where V_P is the peak voltage across the C also called V_C



And $\langle V_L(t)\rangle \cong V_P - 0.5V_R$



FWR with Zener regulation

$V_P = \sqrt{2} \times VAC \times \frac{n_1}{n_2}$ $\quad V_C = V_P - 2V_D$

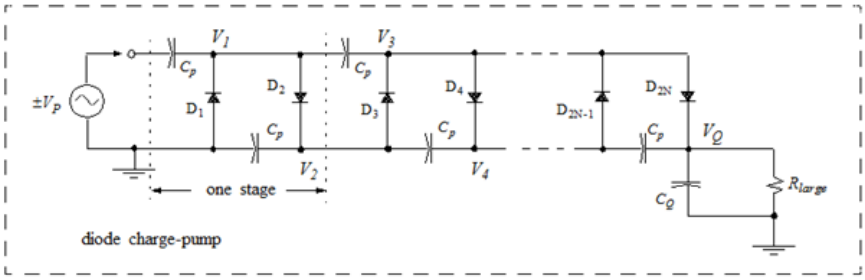
$I_L = P_L/V_L$ $\quad R_L = V_L/I_L$

$R_S = [V_C(min) - V_L]/I_L$

$C \approx 0.5\left(V_C/V_R\right)/fR$ where $R = R_S + R_L$

$\langle P_Z(t)\rangle \cong V_Z \times \left[I_S(\max) + I_S(\min)\right]/2$ where $Is(min)=I_L$, $Is(max) = [V_C(max) - V_L]/R_S$

(c) Diode charge pump



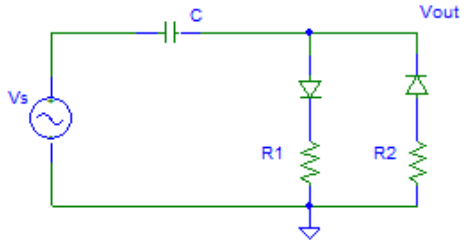
$V_Q = 2N \times (V_P - V_D)$

$I_Q(\max) = 2C_P(V_P - V_D)\, f$

$W_Q = \tfrac{1}{2} C_Q V_N^2 = 2C_Q N^2 V_P^2$

number of cycles to charge C_Q Is $n = N^2 C_Q / C_P$

(d) Adjustable level shifter



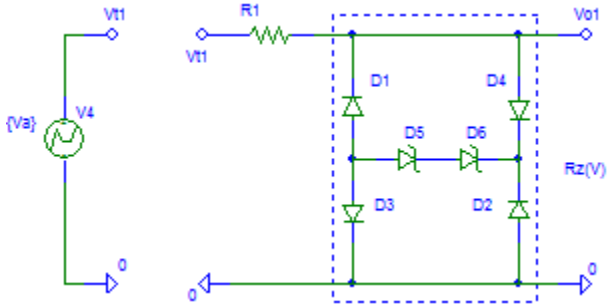
$\alpha_{21} = R_2 / R_1$ for square wave form

$\alpha_{21} \cong (R_2 / R_1)^{1/2}$ for triangle waveform

$\alpha_{21} \cong (R_2 / R_1)^{2/3}$ for sinusoidal

$$\Delta V = (V_P - V_D) \times \frac{(1 - \alpha_{21})}{(1 + \alpha_{21})}$$

(e) Wave-shaping: triangle-wave to sinusoidal



$$V_T = \frac{\pi}{2} \times V_P$$